High Input Impedance Voltage-Mode Universal Biquadratic Filter with One Input and Five Outputs using plus-type DDCCs

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***Abstract*—This paper presents a voltage mode universal biquadratic filter with one input and five output terminals, realizing all the standard filter functions that are high pass, band pass, low pass, notch and all pass, without changing the circuit topology. The proposed circuit employs three plus-type differential difference current conveyors (DDCCs), three grounded resistors and two grounded capacitors. The proposed filter enjoys the features of high input impedance and low active and passive sensitivities. PSPICE simulation results are given to confirm the validity of the proposed circuit.**

***Keywords— active filter, high input impedance, analogue circuits, current conveyors*.**

I. INTRODUCTION

A simple yet useful analog circuit function so often required in communication measurement, and instrumentation system is a biquadratic filter, since it can provide all the standard functions in the same topology [1-2]. There has been a great attention on the design and study of biquadratic analog filter using different current-mode active elements [3]. Voltage mode (VM) biquadratic filter with high input impedance are of great interest because several cells of this kind can be directly connected to implement higher order filters without requiring any other circuitry [8, 13-16, 18-21].

With the increasing interest on the voltage mode universal biquadratic filter with single input and five outputs [7, 11-12, 14-15, 19], there is still need to develop new universal biquadratic filters that offer new advantages. In literature there exist several biquadratic filters based on different active elements [4-21] however; these reported circuits suffer from at least one of the following drawbacks:

- Low-input impedance [4-7, 9, 11-12, 17]
- Excessive use of passive components. [4-5, 7, 13]
- Use of floating capacitor or resistors. [5-8, 11-12, 14-15, 19-20]
- Cannot provide simultaneous, high pass (HP), band pass (BP), low pass (LP), notch (NH) and all-pass (AP) filters. [4, 6, 8-10, 13, 16-18, 20-21]

The literature shows that none of the recently reported works provide all the above features simultaneously. Most of the circuits offer high input impedance and realizes all the standard functions simultaneously from the same topology but one/more passive elements are floating [14, 15, 19]. Recently published circuits in [20] presents cascadable notch/all-pass filters with a feature of high-input impedance and low-output impedances by employing two plus-type differential difference current conveyors [22], two resistors and two grounded capacitors. However it realizes only two standard filter functions.

In this paper, a voltage mode universal biquadratic filter with single input and five output using three plus-type differential difference current conveyor (DDCC+s), three grounded resistors and two grounded capacitors is presented. Moreover, the circuit enjoys high input impedance so that it can be directly connected in cascade to implement higher order filters. With respect to one input and five output circuits in [7, 11-12, 14-15, 19] the proposed circuit employs only grounded passive components, which make it suitable for integrated circuit (IC) implementation and also cancel the effect of parasitic impedances of the active element [23].

II. THE PROPOSED CIRCUIT

The symbol of the DDCC+ is shown in Figure 1, is a five terminal active element, which can be represented by the following matrix equation [22]:

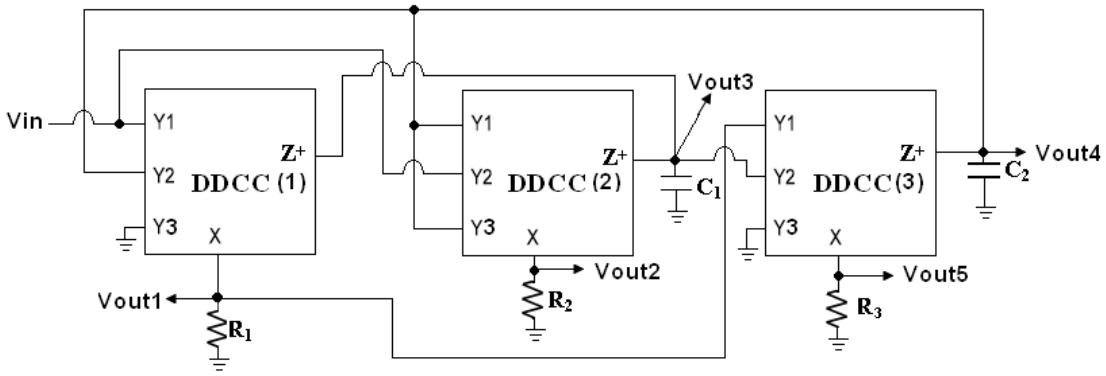

Figure 2. Proposed VM Universal biquadratic filter.

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_Z \\ I_X \end{bmatrix} \quad (1)$$

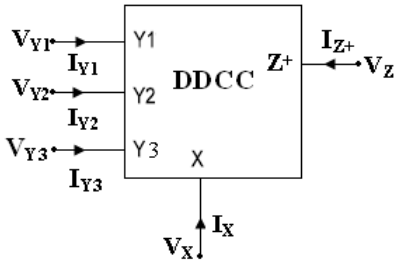

Figure 1. Symbol of DDCC+.

where the suffixes refer to the respective terminals. The voltage at X-terminal follows the voltage difference and addition of terminal Y1, Y2, Y3. The current at terminal Z follow the current at terminal X. It is shown that the ideal DDCC+ exhibits an infinite input resistance at the Y1, Y2, and Y3 terminals. The X-terminal exhibit zero resistance and the Z-terminal exhibit an infinite resistance.

The proposed circuit is shown in Figure 2 by employing three DDCC+s, three grounded resistors and two grounded capacitors. The use of grounded passive components is particularly attractive from the point of IC implementation [23]. A routine analysis of the circuit of Figure 2 yields the following filter transfer functions

$$\frac{V_{OUT1}}{V_{IN}} = \frac{s^2 + \frac{1}{C_1C_2R_2R_3}}{s^2 + \frac{1}{C_2R_3}s + \frac{(2R_1 - R_2)}{C_1C_2R_1R_2R_3}} \quad (2)$$

$$\frac{V_{OUT2}}{V_{IN}} = -\left(\frac{s^2 - \frac{1}{C_2R_3}s + \frac{1}{C_1C_2R_1R_3}}{s^2 + \frac{1}{C_2R_3}s + \frac{(2R_1 - R_2)}{C_1C_2R_1R_2R_3}} \right) \quad (3)$$

$$\frac{V_{OUT3}}{V_{IN}} = \frac{\frac{1}{C_1C_2R_2R_3} + \frac{(R_1 - R_2)}{C_1R_1R_2}s}{s^2 + \frac{1}{C_2R_3}s + \frac{(2R_1 - R_2)}{C_1C_2R_1R_2R_3}} \quad (4)$$

$$\frac{V_{OUT4}}{V_{IN}} = \frac{\frac{1}{C_2R_3}s + \frac{(R_1 - R_2)}{C_1C_2R_1R_2R_3}}{s^2 + \frac{1}{C_2R_3}s + \frac{(2R_1 - R_2)}{C_1C_2R_1R_2R_3}} \quad (5)$$

$$\frac{V_{OUT5}}{V_{IN}} = \frac{s^2 + \frac{(R_1 - R_2)}{C_1R_1R_2}s}{s^2 + \frac{1}{C_2R_3}s + \frac{(2R_1 - R_2)}{C_1C_2R_1R_2R_3}} \quad (6)$$

For $R_1 = R_2 = R$, the equations from (2)-(6) becomes

$$\frac{V_{OUT1}}{V_{IN}} = \frac{s^2 + \frac{1}{C_1C_2RR_3}}{s^2 + \frac{1}{C_2R_3}s + \frac{1}{C_1C_2RR_3}} \quad (7)$$

$$\frac{V_{OUT2}}{V_{IN}} = -\left(\frac{s^2 - \frac{1}{C_2R_3}s + \frac{1}{C_1C_2RR_3}}{s^2 + \frac{1}{C_2R_3}s + \frac{1}{C_1C_2RR_3}} \right) \quad (8)$$

$$\frac{V_{OUT3}}{V_{IN}} = \frac{\frac{1}{C_1C_2RR_3}}{s^2 + \frac{1}{C_2R_3}s + \frac{1}{C_1C_2RR_3}} \quad (9)$$

$$\frac{V_{OUT4}}{V_{IN}} = \frac{\frac{1}{C_2R_3}s}{s^2 + \frac{1}{C_2R_3}s + \frac{1}{C_1C_2RR_3}} \quad (10)$$

$$\frac{V_{OUT5}}{V_{IN}} = \frac{s^2}{s^2 + \frac{1}{C_2R_3}s + \frac{1}{C_1C_2RR_3}} \quad (11)$$

From (7)-(11), it can be seen that a notch (NH) response is obtained from V_{OUT1}, a all-pass(AP) response is obtained from V_{OUT2}, a low-pass (LP) response is obtained from V_{OUT3}, a band-pass (BP) response is obtained from V_{OUT4}, and an high-pass (HP) response is obtained from V_{OUT5}. In all cases, the resonance angular frequency ω_o, the quality factor Q and the bandwidth ω_o/Q are given by

$$\omega_o = \left(\frac{1}{C_1C_2RR_3} \right)^{\frac{1}{2}} \quad (12)$$

$$Q = \left(\frac{R_3C_2}{RC_1} \right)^{\frac{1}{2}} \quad (13)$$

$$\frac{\omega_o}{Q} = \frac{1}{R_3C_2} \quad (14)$$

The input voltage is connected simultaneously to the high input impedance terminals Y1 and Y2 of the DDCC+(1) and DDCC+(2), respectively. So the circuit enjoys the feature of high input impedance. Therefore, it can be used in cascade for realizing higher order filters.

Note that the proposed circuit employs two grounded capacitors at the Z-terminals and three grounded resistors at the X-terminal of the DDCC+. So this circuit offers the feature of direct incorporation of the shunt parasitic capacitance and the series parasitic resistance as a part of the main capacitance and resistance at the Z and X terminals, respectively.

III. Non-Ideal Analysis

Taking into consideration the DDCC+ non idealities, the relationship of the terminal voltages and current can be rewritten as

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} \beta_{k1} & -\beta_{k2} & \beta_{k3} & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \alpha_{k1} \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_Z \\ I_X \end{bmatrix} \quad (15)$$

where $\beta_{kj} = (1 - \varepsilon_{kj})$, for j = 1, 2, 3 and $\alpha_{k1} = (1 - \delta_{k1})$. Also, ε_{kj} and δ_{k1} ($|\varepsilon_{kj}| << 1$ and ($|\delta_{k1}| << 1$) represents voltage tracking error and current tracking error of the DDCC+. β_{k1}, β_{k2}, β_{k3}, are the voltage transfer gain and α_{k1} is the current transfer gain of *the* k-th DDCC+ (k = 1,2,3). Reanalysis of the circuit in Figure 2 that the denominator of the voltage transfer functions becomes

$$D(s) = s^2 + \frac{\beta_{12}\beta_{31}\alpha_{31}}{C_2R_3}s + \frac{\beta_{12}\beta_{32}\alpha_{31}\left[(\beta_{21}+\beta_{23})\alpha_{21} - \alpha_{11}\right]}{C_1C_2RR_3} \quad (16)$$

The non-ideal ω_o, Q and ω_o/Q are given by

$$\omega_o = \left(\frac{\beta_{12}\beta_{32}\alpha_{31}\left[(\beta_{21}+\beta_{23})\alpha_{21} - \alpha_{11}\right]}{C_1C_2RR_3} \right)^{\frac{1}{2}} \quad (17)$$

$$Q = \frac{1}{\beta_{31}} \left(\frac{\beta_{32}\left[(\beta_{21}+\beta_{23})\alpha_{21} - \alpha_{11}\right]C_2R_3}{\beta_{12}\alpha_{31}C_1R} \right)^{\frac{1}{2}} \quad (18)$$

$$\frac{\omega_o}{Q} = \frac{\beta_{12}\beta_{31}\alpha_{31}}{C_2R_3} \quad (19)$$

The active and passive sensitivities of the proposed SIMO voltage-mode filter are derived from eqns. (11)−(12). These are as follows:

$$S^{\omega_o}_{C_1,C_2,R,R_3} = -S^{\omega_o}_{\beta_{12},\beta_{32},\alpha_{31}} = -\frac{1}{2},$$

$$S^{Q}_{C_1,R} = -S^{Q}_{C_2,R_3} = S^{Q}_{\beta_{12},\alpha_{31}} = -S^{Q}_{\beta_{32}} = -\frac{1}{2},\ S^{Q}_{\beta_{13}} = -1,$$

$$S^{\omega_o}_{\alpha_{11}} = S^{Q}_{\alpha_{11}} = \frac{1}{2}\frac{\alpha_{11}}{\left[\alpha_{11} - \alpha_{21}(\beta_{21}+\beta_{23})\right]},$$

$$S^{\omega_o}_{\alpha_{21}} = S^{Q}_{\alpha_{21}} = -\frac{1}{2}\frac{\alpha_{21}(\beta_{21}+\beta_{23})}{\left[\alpha_{11} - \alpha_{21}(\beta_{21}+\beta_{23})\right]}, \quad (20)$$

$$S^{\omega_o}_{\beta_{21}} = S^{Q}_{\beta_{21}} = -\frac{1}{2}\frac{\alpha_{21}\beta_{21}}{\left[\alpha_{11} - \alpha_{21}(\beta_{21}+\beta_{23})\right]},$$

$$S^{\omega_o}_{\beta_{23}} = S^{Q}_{\beta_{23}} = -\frac{1}{2}\frac{\alpha_{21}\beta_{23}}{\left[\alpha_{11} - \alpha_{21}(\beta_{21}+\beta_{23})\right]},$$

$$S^{\frac{\omega_o}{Q}}_{C_2,R_3} = -S^{\frac{\omega_o}{Q}}_{\beta_{12},\beta_{31},\alpha_{31}} = -1$$

From the above sensitivity results it is evident that the sensitivities are low and within unity in absolute value.

IV. SIMULATION RESULTS

To verify the theoretical study, the proposed universal biquadratic filter is simulated by using the PSPICE. The DDCC+ was realized by the CMOS implementation in Figure 3 [24] using 0.5µm, level 3 MOSFET parameters as listed in Table I.The aspect ratio of the MOS transistor are listed in Table II, with the following DC biasing levels V_{dd} = -V_{ss} = 2.5V and V_{bb} = 1.2 V. The proposed circuit is designed for R_1 = R_2 = R_3 = 5 kΩ, C_1 = C_2 = 10 pf with the pole frequency of f_O = 3.17 MHz and a quality factor of Q = 1. The magnitude responses of LP, HP, BP and NH are shown in Figure 4. Figure 5 and Figure 6 shows the magnitude and phase responses of NH and AP of Figure 2. The signal behavior of the proposed circuit is investigated by applying a sinusoidal input voltage with amplitude of 2 V peak-to-peak at a frequency of 3.17 MHz. The time domain input and output signal of the BP response of the proposed circuit is shown in Figure 7. The total harmonic distortion of the output signal at the BP response is shown in Figure 8. The THD is found to be within 5% for a sinusoidal input signal with 2V peak to peak.

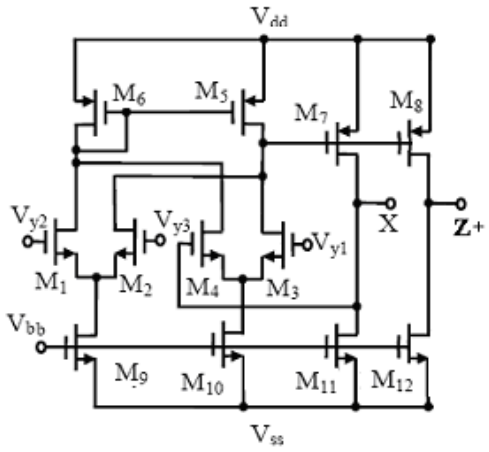

Figure 3. CMOS implementation of DDCC+. [24].

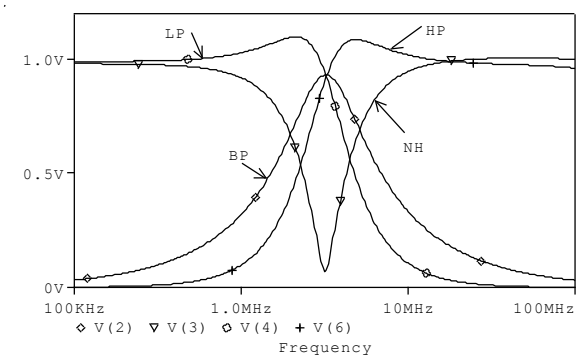

Figure 4. Simulated magnitude responses of the LP, BP, HP, NH at 3.17 MHz of Figure 2.

Table I. 0.5µm LEVEL 3 MOSFET PARAMETERS

NMOS:
LEVEL = 3 UO = 460.5 TOX = 1.0E-8 TPG=-1 VTO = .62 JS = 1.8E-6 XJ = .15E-6 RS = 417 RSH = 2.73 LD = 0.04E-6 ETA = 0 VMAX = 130E3 NSUB = 1.71E17 PB = .761 PHI = 0.905 +THETA = 0.129 GAMMA = 0.69 KAPPA = 0.1 AF =1 WD= .11E-6 CJ = 76.4E-5 MJ = 0.357 CJSW = 5.68E-10 MJSW = 0.302 CGSO = 1.38E-10 CGDO = 1.38E-10 CGBO = 3.45E-10 KF = 3.07E-28 DELTA = 0.42 NFS = 1.2E11
PMOS:
LEVEL = 3 UO = 100 TOX = 1E-8 TPG = 1 VTO = -.58 JS = .38E-6 XJ = 0.1E-6 RS = 886 RSH = 1.81 LD = 0.03E-6 ETA = 0 VMAX = 113E3 NSUB = 2.08E17 PB = .911 PHI = 0.905 THETA = 0.120 GAMMA = .76 KAPPA = 2 AF = 1 WD = .14E-6 CJ = 85E-5 MJ = 0.429 CJSW = 4.67E-10 MJSW = 0.631 CGSO = 1.38E-10 CGDO = 1.38E-10 CGBO = 3.45E-10 KF = 1.08E-29 DELTA = 0.81 NFS = 0.52E11

Table II. DEVICE DIMENSIONS USED IN SIMULATION

Transistors	W/L
M_1, M_2, M_3, M_4	1.6/1
M_5, M_6	8/1
M_7, M_8,	90/1
M_9, M_{10}, M_{11}, M_{12}	20/1

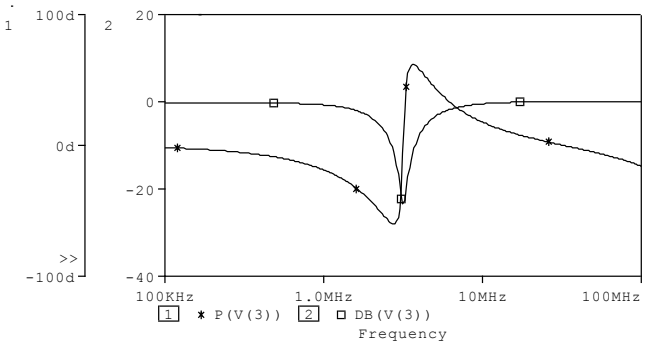

Figure 5. Simulated magnitude and phase response of the NH at 3.17 MHz of Figure 2.

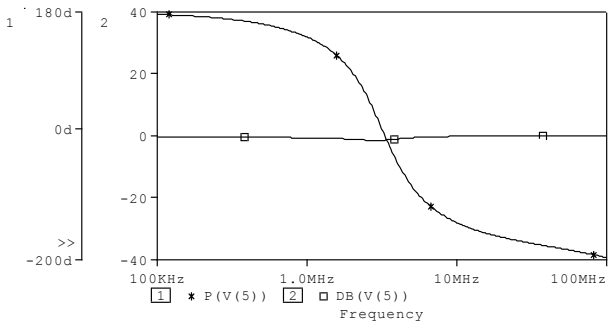

Figure 6. Simulated magnitude and phase response of the AP at 3.17 MHz of Figure 2.

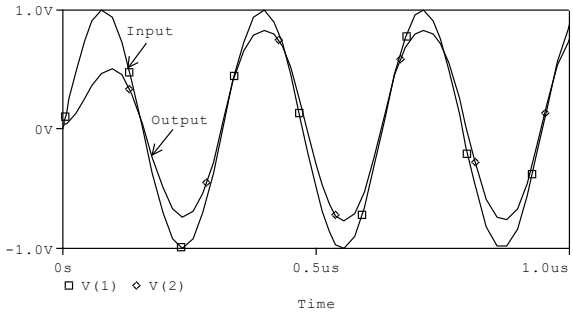

Figure 7 Input and Output signal of the BP response at 3.17 MHz of Figure 2.

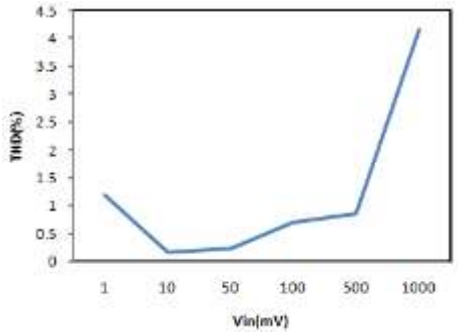

Figure 8 THD variation of the BP response against input voltage at 3.17 MHz.

V. CONCLUSION

In this paper, a high-input impedance voltage-mode universal biquadratic filter with single input and five outputs is presented. The proposed circuit uses three plus-type differential difference current conveyors, two grounded capacitors and three grounded resistors. All the standard filter responses are obtained without changing the passive element. Also the circuit offers the direct incorporation of shunt parasitic capacitances and series parasitic resistances of the DDCC+ as a part of main capacitances and resistances, low active and passive sensitivities and high-input impedance for voltage-mode cascadability.

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