Routing Algorithms for Clos Interconnection Networks.

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***Abstract*— The Clos Interconnection Networks are a class of multistage switching network topologies that provide alternate path between inputs and outputs, making it possible to minimize or eliminate the blocking that can otherwise occur in such networks.**

In this paper, we study the various routing algorithms which have been proposed each imposing extra cost due to hardware use and re-routing algorithm and we also study a routing algorithm which takes blocking avoidance approach for avoiding related costs. There is no blocking while the primary routing is performed from the input to output. The results show that this algorithm is easy than the algorithms previously proposed.

Keywords- Clos Interconnection Networks, Routing Algorithms.

I. INTRODUCTION

Interconnection network plays an important role in parallel processing computers. It is suitable for parallel computers to employ switch interconnection network for connecting processors to shared memory banks or connecting processors to processors in local memory architectures [2]. Furthermore, Clos network [1] is of lower hardware cost than single stage interconnection network (like crossbar). Still, unlike blocking types (like Omega, Baseline, and Butterfly). Clos network is a re-arrange able switched network with none internal blocking.

II. CLOS INTERCONNECTION NETWORK

Using small crossbar switches, Charles Clos [1] introduced a type of interconnection network which is extensively studied and applied as a framework for ATM switches because it is economical, regular, scalable, fault-tolerant and highly efficient. Clos three-stage interconnection networks are intended to be used for data communication and parallel computing system [14].

A switching network is composed of one or more switch stages that can create various paths through creating various connections between their inputs and outputs. Clos three-stage network is an example of multistage switching network Figure 1.

Clos Interconnection Networks [1] have been gaining attention due to their positional uses in data networks and computing systems. The three-stage Clos network consists of two symmetrical outer stages of rectangular switches, with an inner stage of square switches. The first stage of a three-stage network is called Input stages which contain r switches, each of which has n inputs and m outputs. Each switch is a simple crossbar switch which can realize any mapping of its Input on to its output on a one-to-one basis. The second stage is called middle stage consists of m (r×r) switches, each of which receives exactly one input from each first-stage switch. The third stage is called output stage has r (m×m) switches, each of which receives exactly one Input from each Second stage switch. The number of Inputs to the clos network is N=nr and m≥n. As C(n,m,r) known all possible permutations between Inputs and outputs. A link can be accessed between stages provided it is usable and not engaged.

This study presents the routing mechanism in clos Interconnection networks, taking blocking-avoidance approach. The rest of the paper is organized as follows: Section 2 introduces the routing algorithms for clos networks, Section 3 presents a blocking avoidance approach for clos networks and Section 4 summarizes the paper.

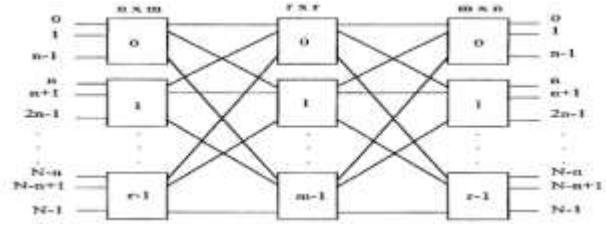

Figure 1. A Basic General Clos Interconnection Network

III. ROUTING ALGORITHMS

Limited by the high time complexity of its routing algorithm, Clos network can't be widely utilized in parallel

processing system. To this issue, various routing algorithms for clos network have been presented which are reported in the literature [3] [13].

Routing algorithm can be divided into two groups: 1- Blocking avoidance approach, 2- Routing irrespective of blocking. In the first method, routing in the algorithm is performed in such a way that there is no blocking but in the second method, initially the routing is performed from input set to output set. In case of any blocking, attempts are made to eliminate it through changing the arrangements in network switching, using routing algorithm [14].

All routing algorithm in multistage connection can be performed by 2 method 1-Graph Coloring Algorithm 2-Decomposition algorithm using matrix. In general, matrix decomposition is not as fast as graph coloring algorithms in the computational complexity. However, as the network size is too large, it will be inefficient. Decomposition algorithm using matrix has the following advantages: Direct locating the problems and enjoying simplicity in switching settings.

A. *Neiman's Algorithms*

Unfortunately, it has been shown that many of the early matrix decomposition algorithms are incomplete except Neiman's Algorithm, which is correct in principle, but give no details for implementation and has the time complexity $0(N\sqrt{N})$ [8].

B. *GS Algorithm*

Gordon and Srikanthan et. Al. [7] introduced an algorithm, referred to as the (GS) algorithm [11] which uses two nouvelle matrix called the specification matrix and the count matrix (the count matrix is not strictly necessary but helps in describing the algorithm). But the GS algorithm is suspected to lead the infinite looping.

C. *GS Modified Algorithm*

Later, a new method called the modified methods of GS was proposed. This algorithm was proposed at time complexity $0(N\sqrt{N}\log\sqrt{N})$, by adding 3 steps to the main algorithm and deleting 2 steps for the purpose of eliminate indefinite loops [11].

D. *Heuristic Algorithm*

Heuristic Routing Algorithm using minimum distribution priority scheme was introduced for routing clos networks. This algorithm can achieve full non-deadlock routing and also this method had the capability of accessing all non-blocking routings, reducing its time complexity to $0(N\sqrt{N})$ in the worst situation [13].

IV. Blocking Avoidance Routing Algorithms For Clos Networks

It is customary to assume that the necessary connections involve every input and every output, and thus are represent able by a permutation:

P= 0 1----------i----------N-1
Π(0) π(1)----------π(i)----------π(N-1)

Where input i is connected to output π(i), $0 \le i \le N-1$, N=nr. Since each switch between input and output is assumed to be non-blocking. P can be changed between Input and output switches [8].

In this algorithm, the matrix is used in such a way that network is initially has its connections. Then the new inputs are added into the network in such a way that there will be not any blocking. This is made possible through 4 main matrix (W, X, Y, Z) and a single-dimensional array(e). The matrix consists of elements 0, 1. 0 represents the free link and 1 represents the engaged link in the network [14].

Now the matrix and array(e) are explained briefly as such defined below step by step:

1. Matrix W represents a connection between input switches and inputs of each input switch. The number of rows (i) represents input switches and the number of columns (j) represents the input of each input matrix.
2. Matrix X represents the connection between middle switches and input of each middle switch. The number of row (i1) represents the middle switches and the number of column (j1) represents inputs of each middle switch.
3. Matrix Y represents the connection between output switches and inputs of each output switches. The number of rows (i3) comprises output switch and the number of column (j3) represents the input of each output switch.
4. Matrix Z represents the connection between the output of each output switch and output switches. The row (i4) represents output switches and column (i4) represents the outputs of each output switch.
5. Array (e) each member of this array represents the number of the engaged input of each middle switch. The length of the array equals the number of middle stages.

V. Description Of Algorithm

Step 1). Initialize by Setting Matrix(X), Matrix(Y), Matrix(Z) and array(e)= null.

Step 2). Read Input Matrix(W).

Step 3). For each of row elements of Matrix (W), that is "True", if (W[i,j]==1) then {Find the First column elements of Matrix X, that is "False", if ($X[i_1,j_1]$==0) {Swap (W[I,j], $X[i_1,j_1]$:}}

Step 4). For each of row elements of Matrix X, that is "True", if ($X[i_1,j_1]$==1) then {S++;}e[k++]=S; if (e[k>0]) then { $X[k][j_{11}] = 1$, k--;}

Step 5). For each of row elements of Matrix (X), that is "True", if ($X[i_1,j_1]$==1) then {Find the First row elements of Matrix Y, that is "False", if ($Y[i_3,j_3]$==0) {Swap ($X[i_1,j_1]$, $Y[i_3,j_3]$:}}

Step 6). For each of row elements of Matrix (Y), that is "True", if (Y[i_3,j_3]==1) then {Find the First row elements of Matrix Z, that is "False", if (Z[i_4,j_4]==0) {Swap (Y[i_3,j_3], Z[i_4,j_4]:}}

As you can see, all elements in matrix W, X and Y can be transferred to the next stage matrix in a parallel manner. This speaks for the parallel routing in the proposed manner.

VI. Analysis And Comparison

This algorithm eliminates the blocking and each of its iteration steps is implemented for constant times. The following should be taken into account to compute the complexity of routing algorithm.

1, m = n, this indicates that the number of middle stage switches (m) equals the number of input ports of the switches of input stage (n).

2.N=r×n, this indicates that overall network inputs are obtained by multiplying the number of switches of input stage (r) by the input ports of each switch of input stage (n).

3.n = √N

Each matrix is read by time O(N) and the main body of algorithm is formed at 0(Nn). Thus, the overall complexity of proposed algorithm is:

$$O(Nn) + 3O(N) = O(Nn)=O(N\sqrt{N})$$

TABLE I. Shows The Complexity of Blocking-Avoidance Algorithm, Drawing On The Previously Proposed Algorithms

Algorithm name	Complexity of Routing Algorithm
GS Algorithm	N√N
GS Modification Algorithm	N√Nlog√N
Heuristic Algorithm	N√N
Blocking- Avoidance Algorithm	N√N

In GS routing Algorithm, there are indefinite loops which don't appear in the proposed routing Algorithm in this study and resulting in higher efficiency.

In Heuristic routing Algorithm, rearrangement is required. This lead to additional hardware cost. While, in blocking avoidance approach, there is no such cost.

Hence, this method gives better performance than other methods.

VII. Conclusion And Future Work

This study presents a routing Algorithm for Clos Interconnection Networks, taking a blocking-avoidance approach so that the routing is performed properly from input to output without blocking the links in network. While the previously proposed Algorithm, the strictly non-blocking network was defined by simple routing this results in high hardware costs. The method proposed by this study has solved the problem. This algorithm completes its cycle at time complexity o(N√N). These types of routing are usually used in data transmission networks for the purpose of reducing the delay in transmission. The future studies can examine the way in which new algorithms can be used to reduce routing time and the use of memory and to reduce the complexity of the algorithms.

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