Design and implementation of DPLL using 1.2µm CMOS Technology

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***Abstract*—Due to ever rising growth of wireless communication systems, the need for low power and cost effective devices is growing exponentially. The Phase locked loops (PLL) are the fundamental circuit elements of data transmission systems and have wide applications in data modulation, demodulation and mobile communication. Voltage control oscillators (VCO) are the critical and necessary building blocks of these PLL systems. In This paper the design and analysis of digital phase locked loop (DPLL) has been discussed. Phase locked-loops (PLLs) are widely using to generate well-timed on-chip clocks to be used in high-performance digital systems.**

The design is applied to the T-SPICE simulation program; implemented in a 1.2µm CMOS technology and at 5V supply voltage to operate VCO at a frequency of 987.6 KHz with a delay time of 202.49965ns.

***Keywords*- VCO, DPLL, Phase frequency detector, Loop filter.**

I. INTRODUCTION

In high speed communication systems, to make sure clock recover and synchronization via PLL is a most important factor of the systems, while in digital signal processing circuit, frequency synthesizer consisting of digital phase-locked loop has become a key part which is used for system clock inside chips. Phase locked loops (PLLs) are widely used in microprocessors and digital systems for clock generation and frequency synthesizers.

The phase lock loop is a used to generate an output signal in the phase of the reference signal [1]. This is achieved after many iterations of comparison of the reference and feedback signals. If reference and feedback signal are not in phase, the phase frequency detector produces an error signal. If both the signals are in same phase then the error signal will be zero and the output of the PLL is constant. This mode is called as locked mode. The PLL circuit continues to compare the two signals but because they are in lock mode, the PLL output is constant.

The basic digital PLL has following three fundamental functional blocks [2, 3].

1. A Phase frequency Detector (PFD)
2. A Loop Filter (LF)
3. A Voltage Controlled Oscillator (VCO)

The circuit formation of DPLL is shown in figure 1:

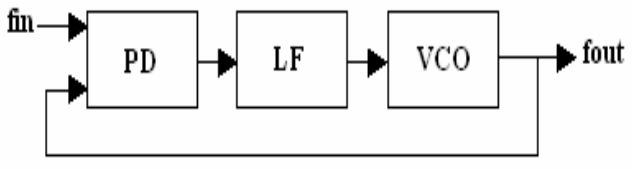

Fig. 1: Block Diagram of basic digital PLL block diagram

The input signal frequency or reference frequency of phase frequency detector 'f_{in}' is compared with the VCO frequency 'f_{out}' to produce an error voltage, which is proportional to the phase difference or frequency difference of these two signals. The error voltage is then filtered and applied to the VCO. The control voltage of the VCO changes the frequency in a direction of the phase difference between the input signal and the local oscillator. It helps to reduce the difference voltage. When input and output signals are synchronized, the PLL is said to be in lock mode. When the PLL is locked, the control voltage is such that the frequency of the VCO is exactly equal to the average frequency of the input signal. if the initial difference between the input signal and the VCO is less, the PLL finally locks on to the input signal. This period of frequency acquisition, is referred as pull-in time, and it can be very long or very short, depending on the bandwidth of the PLL.

II. ARCHITECTURE OF CHARGE PUMP PHASE LOCKED LOOP

A charge pump PLL consists of four fundamental components rather than three components used in the basic PLLs [3, 4]:

1. Phase frequency detector (PFD)
2. Charge pump (CP)
3. Loop filter (LF)
4. Voltage controlled oscillator (VCO)

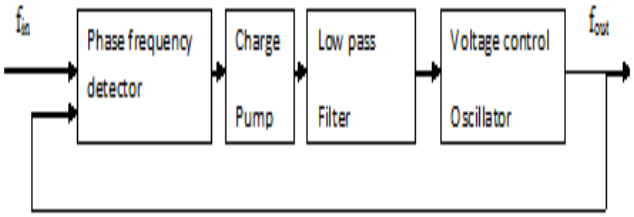

Fig. 2: Block Diagram of charge pump PLL diagram

The circuit performance of charge pump PLL is shown in figure 2.The difference signal is the input signal to the charge pump. By this charge pump current, the magnitude of charge stored in the loop filter is to be controlled [2, 5].

- The Loop Filter is basically a low pass filter, it pass the low frequency component and minimizes noise in the signal with the maximum response time. The passive low pass loop filter is used to convert back the charge pump current into the voltage.
- Voltage controlled oscillator (VCO) is a nonlinear device, which produces an output signal whose frequency is controlled by the loop filter voltage.

A. *Phase Frequency Detector (PFD)*

The first block of charge pump PLLs incorporates sequential-logic, named as PFDs have being used commonly in recent years [5]. The Phase Frequency Detector is also called a phase comparator.

The PFD design uses two flip flops with reset features [6]. It can detect a difference in phase and frequency between the reference and feedback signals. The circuit of phase frequency detector is shown in figure 3, in which two positive edge triggered D flip flops and one AND gate is used. Two inputs of the flip flop are connected to V_{DD} and clock inputs A and B are connected to data and d-clock respectively. The outputs of the PFD are two control signals called UP and DOWN. If both the outputs of flip flops, Q_A and Q_B are high, the AND gate produces a high output which reset the two flip flops. If data frequency 'f_{in}' is higher or leading the output frequency 'f_{out}', the Up signal is generated and when f_{in} is lower or lagging the 'f_{out}', then the DOWN signal is activated [6,7]. The Up and Down pulses are shown in the Figures 4 (a) and (b). The circuit Simulation diagram of PFD and its output waveforms are shown in the figure 5 and figure 6 respectively.

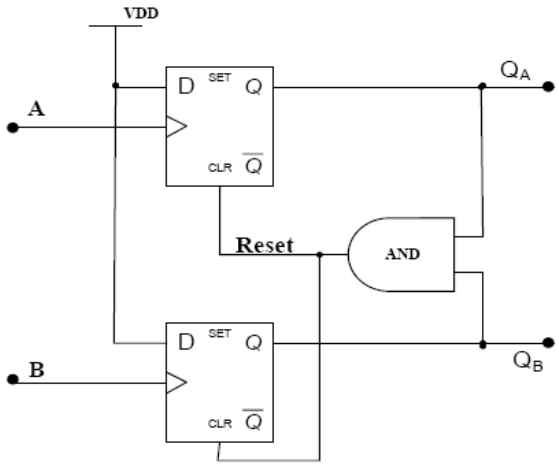

Fig 3: The Block Diagram of Phase Frequency Detector.

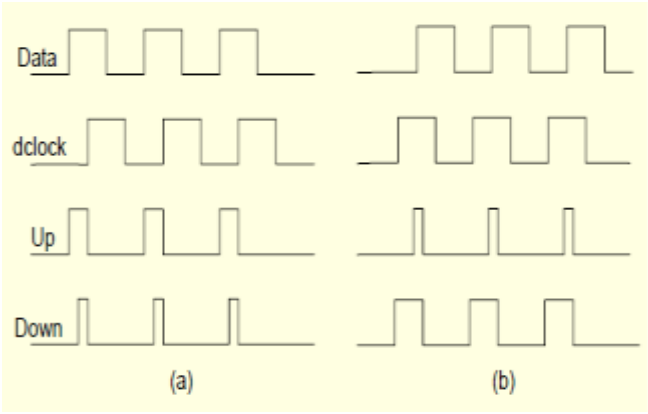

Fig. 4:Up and Down signal Generation (a) Up signal (b) Down signal

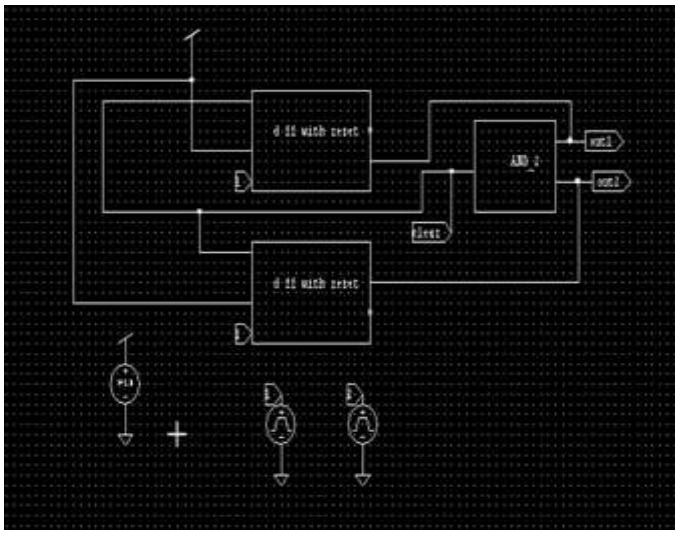

Fig. 5: Circuit Simulation diagram of PFD

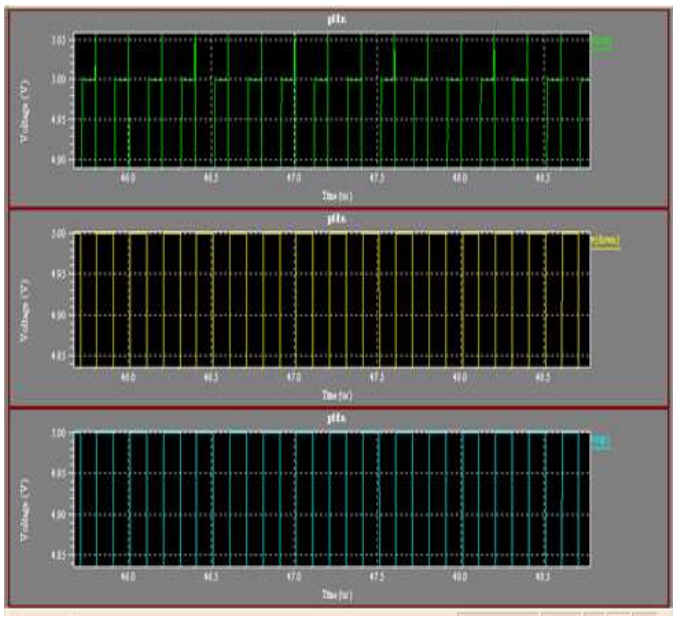

Fig.6: Output waveform of PFD

B. *Charge Pump*

The circuit of Charge pump is used to combine both the outputs of PFD and gives a single output which is fed to the input of the filter. It converts output of the phase frequency detector into voltage signals which are directly proportional to the phase difference of the PLL inputs used to tune the VCO [4, 7, 8].

The Charge Pump converts the Up and Down pulses of the PFD into a DC voltage. It gives a constant current. The amplitude of the current always remains same but the polarity changes which depending upon the value of the Up and Down signal.

The combination of PFD, Charge pump and loop filter is shown in figure 7. Table I shows the analysis of three state of charge pump with charging or discharging current of Capacitor. The CP either charges or discharges the capacitor in the LF. It means the CP generates the control signal by adding or removing charges in the Low pass Filter [7, 9]. The timing diagram of charge pump is shown the Figure 8. The diagram shows the output with respect to inputs A and B.

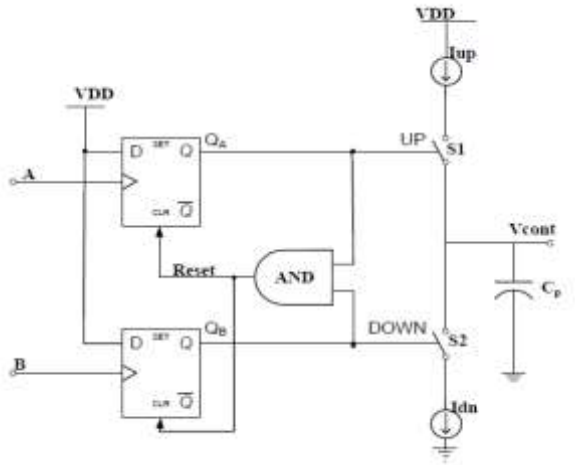

Fig 7: Combined Circuit of PFD-CP-Loop Filter

TABLE I
Four state of the Charge Pump

UP Signal	DOWN Signal	Condition	Note
1	0	Charging	I_{charge} flows into filter
0	1	Discharging	$I_{discharge}$ flows out from filter
0	0	V_{ctrl} remain constant	$I_{charge} = I_{discharge} = 0$
1	1	V_{ctrl} remain constant	$I_{charge} = I_{discharge} \neq 0$

C. *Loop Filter*

The loop filter is basically a low pass filter. The basic function of the loop filter is to provide a filtering action on the charge pump output signal. The higher frequency terms can be eliminated and lower frequency terms are produced due to the phase detector action. Generally, in the steady (or locked) state, the output of loop filter is a stable voltage which is suitable for the control of VCO. It is used to integrate the current pulses that flow from/ to the charge pump and convert them to control voltages. The output voltage of the loop filter controls the oscillation frequency of VCO.

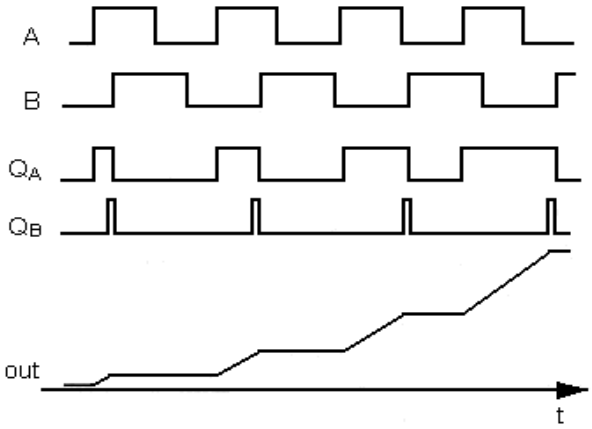

Fig.8: PFD with charge pump timing diagram

A first order loop filter (Figure 9) uses 300KΩ resistance and 10pF capacitor. The gain of the loop filter can be calculated using equations are as follows. The cut-off frequency of this filter is denoted by f_c.

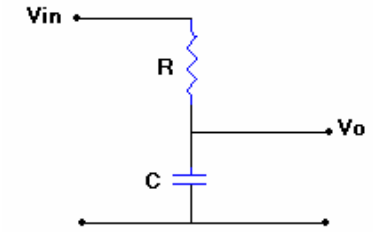

Fig.9: Circuit of 1st order Low Pass Filter

$$Vo = \frac{\frac{1}{j\omega RC}}{\frac{1}{j\omega RC}+R} \text{ Vin}$$

$$\text{Vo} = \frac{1}{j\omega RC+1}\text{Vin}$$

The expression of cut-off angular frequency is given as

$$\omega_c = \frac{1}{RC}$$

Using parameters of the filter the cut-off frequency is given as

$$f_c = \frac{1}{2\Pi RC}$$

f_c = 53.07MHz

D. *Voltage Controlled Oscillator (VCO)*

The principle of the voltage-controlled oscillator is to produce a periodic output signal whose frequency is proportional to its input voltage. The output frequency of VCO approximately has a linear proportion with the input voltage from the loop filter. Hence, by changing the applied voltage to the VCO, the output frequency of the VCO can be changed [11, 12, 13].

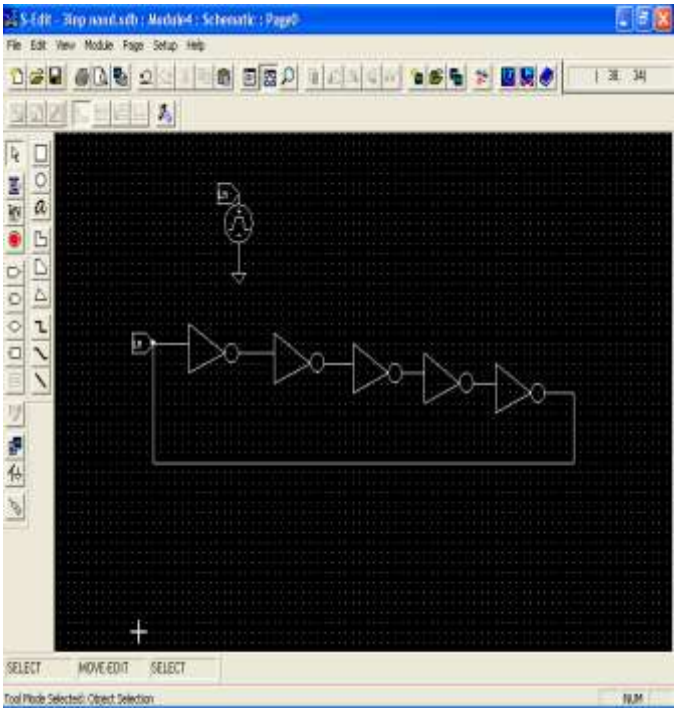

Fig.10: CMOS five stage Ring Oscillator

The VCO has been implemented using a 5-stage CMOS ring oscillator shown in figure 10. A ring oscillator is chosen due to the easiness of design and implementation. The Ring oscillator has a wide tuning range, a high oscillation frequency, low power consumption and occupies small area, but it has poor phase-noise performance as compared to LC oscillator circuit.

The frequency of oscillation is controlled by the applied dc voltage, the frequency or phase modulation is caused by feeding modulating signals into the VCO.

The frequency of oscillation is given as expression of:

$$f_{osc} = \frac{1}{T} = \frac{1}{nt_d} \quad \ldots 4$$

Where,

t_d is the propagation delay per stage, and N is the number of inverter stages in ring oscillator.

III. 987.6KHz-5V VCO DESIGN

The delay of single CMOS inverter is about 202.5ns .The total time delay of five stage ring oscillator is about 0.2 ns that are listed in the Table II.

TABLE III

VCO design parameters

Parameter	**Value**
Center frequency	987.6KHz
No. of inverter stage	5
Inverter delay	202.49965ns
t_{PLH}	0.0333ns
t_{PHL}	404.966ns
5 stage inverter delay	1.01ps

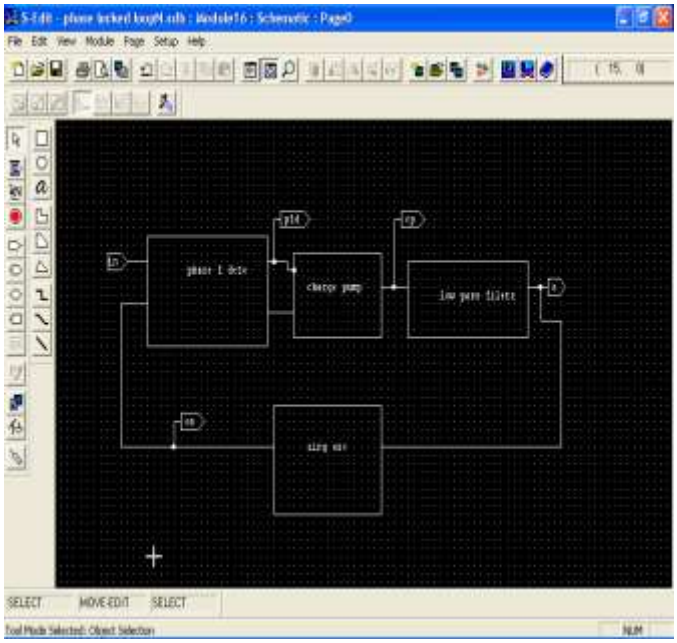

Fig. 11: A typical PLL block diagram

Figure 11 shows the complete block diagram of digital PLL. The output of the VCO is fed back to the PFD and compared with the reference frequency. When both the frequency becomes equal; the output of the PLL is said to be locked.

IV. SIMULATION AND RESULTS

The PLL has been simulated by using 1.2 micrometer CMOS technology with a supply voltage of 5V. The delay time of the ring oscillator is about 202.5 ns. The graph of the output frequency of VCO is shown in figure 12. After establishing T-spice model for all the essential blocks, the complete simulated output waveforms of digital phase lock loop is shown in figure 13. By the graph, the output voltage v(o) of low pass filter is reset to almost zero volts at 8.5 µsec, after that the correct output will be obtained. The oscillating frequency of VCO changes its value whenever the plus or minus signal is available.

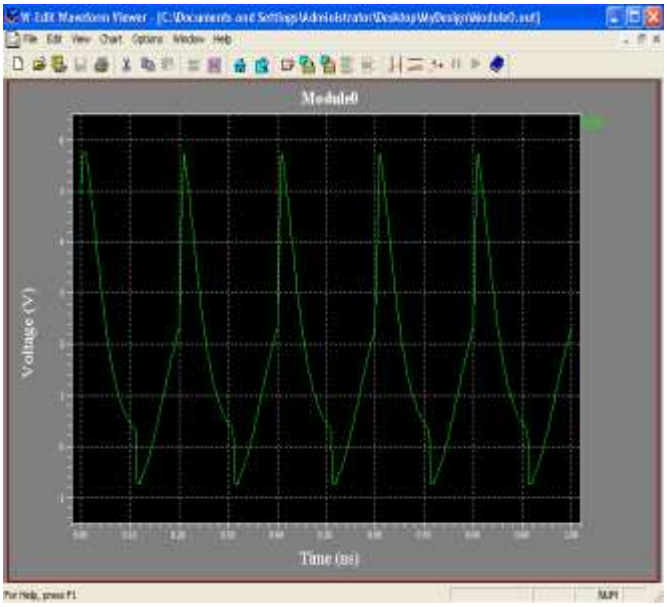

Fig. 12: 987.6KHz Frequency for COMS ring oscillator

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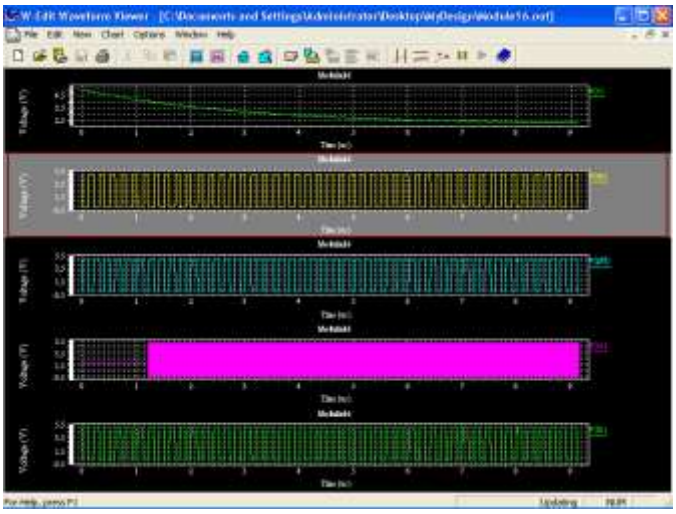

Fig. 13: The simulated output waveforms of complete DPLL

IV. CONCLUSION

The PLL design by this method has a high performance due to accuracy in progress. This can significantly improve the PLL applications such as frequency synthesizer, which is widely used in high-speed data processing. It usually implemented by PLLs because of low implementation cost and excellent noise performance. The design of Voltage Controlled Oscillator (VCO) was implemented using a 5-stage ring oscillator. In this work a PLL with an improved lock time is presented. The lock time of the PLL is found to be 1.21µs. The lock time of the PLL generally depends upon the type of PFD architecture used in the circuit and the parameters of the charge pump and loop filter. Therefore by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values a better lock time can be achieved. The designing of the loop filter was chosen to be simple. By applying more than 20 pF capacitor the control voltage of VCO change slowly. Because of this large valued capacitor, the lock-in time is a little long (about 10µs). Designing a more complex filter, the lock-in time may be shorter.

A high speed phase frequency detector, charge pump and second order low pass filter as loop filter is designed with 1.2µm CMOS technology , 5v power supply and 987.6KHz input frequency. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values we can achieve a better lock time. The Spice simulation program shows the satisfactory results of this work.

V. REFERENCES

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