Comparative Performance Analysis of Various PPM Adders

Vimal Kant Pandey
Electronics and Communication
Dehradun Institute of Technology,
Dehradun, India
vimalpandey94@gmail.com

Rajeev Kumar
Electronics and Communication
Dehradun Institute of Technology
Dehradun, India
rajeevkrc@gmail.com

***Abstract*- This paper presents a comparative study of different redundant binary full adders (Plus-Plus-Minus (PPM) adder). These PPM adders are simulated to evaluate their performance in total power dissipation, speed and PDP. The performances of these circuits are based on 180nm process model at a supply voltage of 1.8V. We also proposed a new design for PPM adder using 13-transistors. The simulation results reveal that the proposed design is more power, area efficient and faster than the best available PPM circuit in the literature.**

***Keywords*- PPM adder; redundant binary adder; high-speed; low-power;**

I. INTRODUCTION

The conventional operations like addition, subtraction and multiplication, can produce the carry-propagation chains. In the late 1950, Aviziens[1] introduced the redundant number system to solve this problem. The important properties of this number system are to have more than one representation for its value and to represent negative numbers easily. Redundant binary (RB) number representations are used extensively to speed up arithmetic operations within both in sign processing and other applications with moderate frequency of arithmetic operations. PPM adder is used as the basic building block in RB system to handle the signed digit operations. Thus, improving its performance is critical for enhancing the overall performance of RB-based DSP systems.

PPM adders are based on the Redundant Binary (RB) number system, which differs from conventional binary number system in that the individual digit of an RB number, can represent more than two values (binary 0 and 1). A radix-2 redundant signed-digit number system is based on a digit set S ={1,0,-1} , where each digit can assume any of the three values from the set S instead of just the two values, 0 and 1, as in standard binary number system. Consequently, redundancy is introduced in the number system. Such representation is very advantageous while designing high speed systems, since it allows "carry-free" addition [1-3]. In redundant binary signed digit number system, the signed-digit operation is taken care of by the PPM adder and consequently there is no need for an explicit mechanism to handle signed digit number.

In this paper, we carry out a comprehensive study of different efficient designs of the PPM 1-bit adders, using different number of transistors, for redundant number system applications. We also propose a new design for the PPM adder using XOR-XNOR gate. The rest of the paper is organized as follows: In section II, basics of PPM adders are discussed. In section III, different designs of PPM adders are discussed. In section IV, the proposed design of PPM adder based on XOR-XNOR [4] circuit is presented. In section V, simulation results for proposed and existing designs of PPM adder circuits are given and comparisons are carried out.

II. PPM ADDER BASICS

A PPM adder [5]-[6] performs the addition of a redundant number x (where, x= x+- x-) to an unsigned binary number y, resulting in another redundant number expressed by an interim sum u- and a transfer digit t+. The input bits are defined as x+, x-, y ε {0, 1} and the output bits are t+, u- ε {0, 1}.

The PPM adder shown in figure 1 performs the following operations:

$$x + y = x^{+} - x^{-} + y = 2t^{+} - u^{-} \quad (1)$$

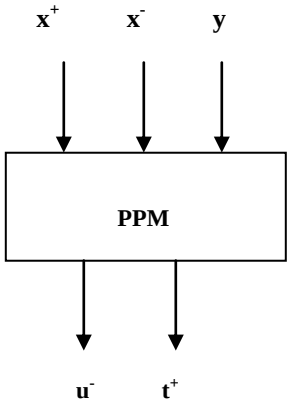

Figure.1 Block Diagram of PPM Adder

Where x is redundant number expressed as:

$$\mathbf{x = x^+ - x^-} \quad (2)$$

Therefore, $\mathbf{x^+ - x^- + y = 2t^+ - u^-}$ (3)

Encoding of digit x, using radix-2 redundant number system is given in Table 1.

TABLE 1: ENCODING OF THE DIGIT X

X	X^+	x^-	$X = x^+.x^-$
0	0	0	00
-1	0	1	01
1	1	0	10
0	1	1	11

Using the truth table the interim sum u^- and the transfer digit t^+ can be expressed by the following Boolean expression:

$$u^- = (x^+)'(x^-)\,y' + (x^+)'(x^-)'y + (x^+)\,(x^-)'y' + x^+x^-y \quad (4)$$

$$t^+ = (x^+)'(x^-)'y + (x^+)\,(x^-)'y' + (x^+)\,(x^-)'y + x^+x^-y \quad (5)$$

III. DIFFERENT PPM ADDERS TOPOLOGIES

Full adders are designed targeting a reduction in the power consumption, time delay and chip area. Therefore, reducing the number of transistors in a PPM Adder, from more than 20 [1], [7], [8] to 16 transistors (16-T) or less, without compromising its performance is presented in this paper.

24-transistors (24-T) PPM adder design [7] is shown in Fig.2. This technique is popular and produces results that are widely accepted one but it requires more numbers of CMOS transistors. Since it has a large number of transistors, both power dissipation and time delay are high. The advantage of this design style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage and arbitrary transistor sizes. This circuit can operate with full output voltage swing.

Two variations of 14-transistors (14-T) PPM adder design [9], called set-1 and set-2, are shown in Fig. 3 and Fig. 4 respectively. Set-1 adder is based on sharing method (part of the circuit is shared to generate the two outputs) and the generation of one output depends on the other output signal. Set-2 design is derived from a new algorithm, where both output bits are generated simultaneously (called balanced method). Based on the truth table, the logic functions of u^- for the set-1 and set- 2 of the PPM adder is obtained as:

$$u^- = (x^+ \overline{\oplus} x^- \overline{\oplus} y)$$

Thus, the output u^- can be generated by using two XNOR gates. The generation of t^+ for the set-1 PPM adder is obtained from Fig. 3 as

$$t^+ = x^-(x^+ \oplus y) + y(x^+ \overline{\oplus} y)$$

The second set (set-2) (Fig. 4) of PPM adder is better than the first set (set-1) of PPM adder, with a balance generation of the output signals u^- and t^+. The resultant improvement is due to the fact that the generation of signal t^+ does not depend on the signal u^-. Based on the truth table, the logic function of t^+, for the set-2 of the PPM adder, is obtained as

$$t^+ = x^+(x^+ \oplus x^-) + y(x^+ \overline{\oplus} x^-)$$

Further improvement of the 14-T (set-2) PPM adder is a 16 transistors (16-T) PPM adder shown in Fig. 5.

The PPM adder [14] is shown in Fig. 6 is an improvement of 16 transistors PPM adder. This circuit provides good output voltage levels for all combination of input because of the availability of feedback PMOS and NMOS transistor loop. The circuit has two cross-coupled PMOS and NMOS transistors connected between XOR and XNOR outputs. This arrangement eliminates the output threshold voltage loss, improve the noise immunity and enhance the driving capability of the circuit. To overcome the problem of skewed outputs the XOR and XNOR functions are combined in one circuit as shown in Fig. 6. The circuit has a single connection to VDD and single connection to GND. The existence to single VDD and GND connections improves the driving capability of the circuit [10]-[13].

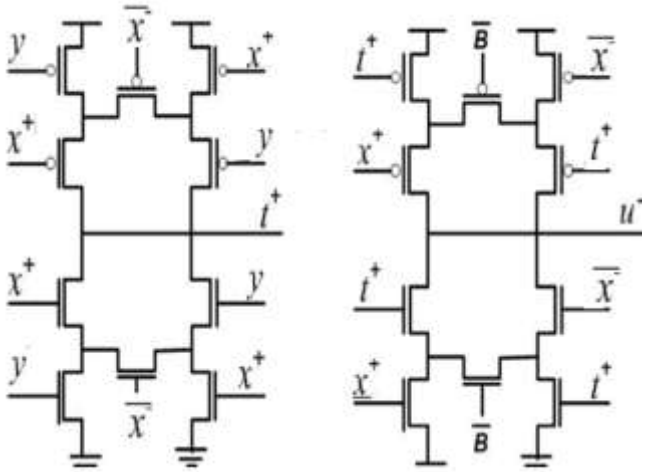

Figure.2. 24-T PPM Adder [7]

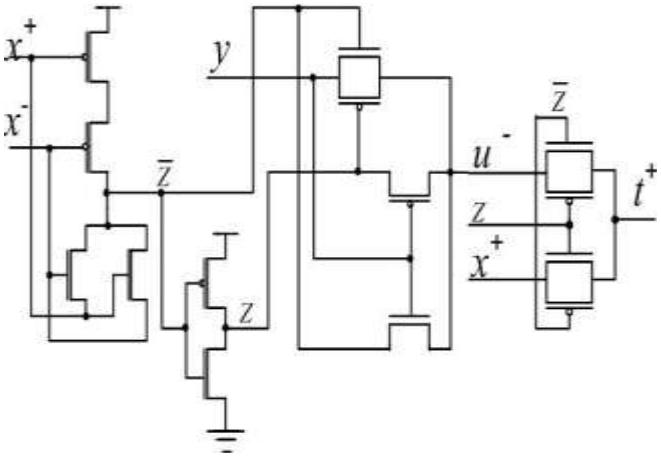

Figure.3. 14-T (set 1) PPM Adder [9]

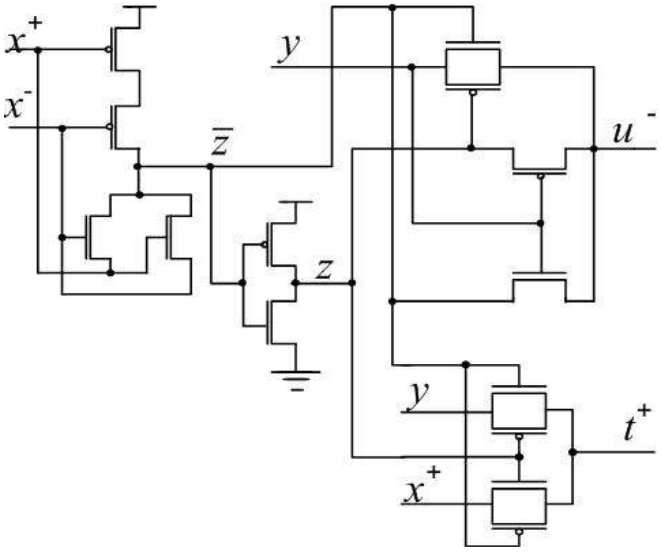

Figure.4. 14- T (set 2) PPM Adder[9]

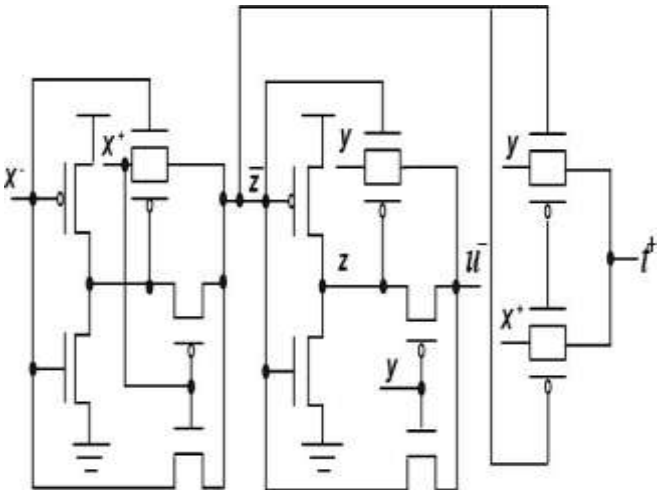

Figure.5. 16-T PPM Adder

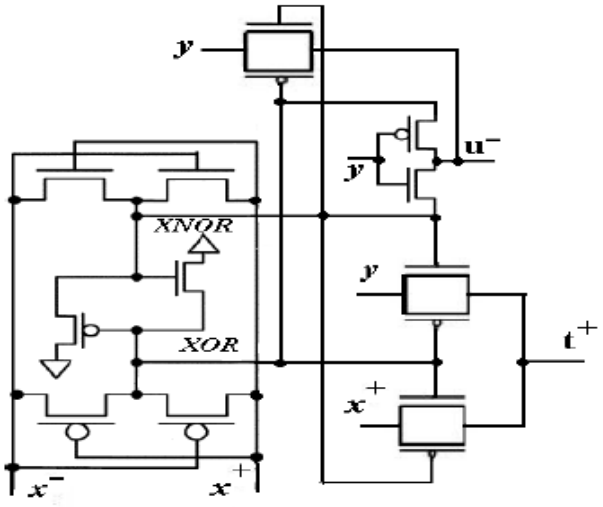

Figure.6. 14-T PPM Adder [14]

IV.PROPOSED PPM ADDER CIRCUIT

The proposed PPM adder circuit is shown in below Fig. 7. From the equations of u^- and t^+ it is clear that the PPM adder can be designed by using XOR-XNOR circuits. We are using the XOR-XNOR circuit [4] consisting of 5-transistors. The proposed circuit consist of 13-transistors and has better performance compared to the best available circuit of PPM adder discussed in the paper.

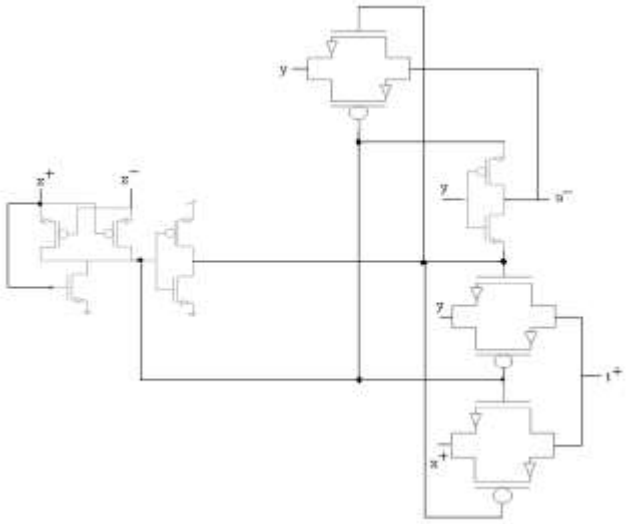

Figure.7 Proposed 13-T PPM Adder circuit

V. SIMULATION RESULTS AND COMPARISON

The power dissipation and the time delay of the proposed PPM adders and all reported circuits are computed when implemented in 0.18µm CMOS technology and supply voltage of 1.8V. To perform comparative study of various adder circuits same input pattern is applied to all circuits. A constant output load capacitance of 10fF is used for the power and delay measurements.

The delay is measured between the time when the changing input reaches its 50% voltage level to the time when the resulting output reaches its 50% voltage level for both rise and fall output transitions.

The comparative performance of various PPM adder circuits at 1.8V supply voltage is given in Table II.

TABLE II. COMPARATIVE PERFORMANCE OF VARIOUS PPM ADDERS

PPM Adder	Delay (nsec)	Power (µW)	PDP
24-T PPM	0.159	31.45	5.00055
14-TPPM (set-1)	0.107	13.25	1.41775
14-T PPM (set-2)	0.071	14.01	0.99471
16-T PPM	0.027	124.23	3.35421
14-T PPM	0.022	13.12	0.28864
Proposed PPM Adder	0.0127	13.41	0.17031

VI. CONCLUSIONS

This study is the comprehensive study of the PPM adder designs. Different PPM adder designs were analyzed based on a sharing and balanced format derived from the PPM addition equation and its corresponding truth table. Based on the implementation results of 0.18um CMOS technology, the proposed 13 transistor designs have lower power consumption and higher speed while requiring fewer transistors compared to the previously published PPM adders. The proposed new designs can be widely used for computer arithmetic units in redundant binary systems and other applications.

REFERENCES

[1] Avizienis, "Signed digit number representation for fast Parallel arithmetic," IRE Transactions on Electronic Computers, vol. EC-10, pp. 389-400, Sept. 1961.

[2] B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, Oxford: Oxford University Press, 2000.

[3] K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation. New York: John Wiley & Sons, Inc., 1999.

[4] R. Kumar. V.K. Pandey, "A New 5-Transistor XOR-XNOR Circuit Based on the Pass Transistor Logic", 978-1-4673-0125-1, pp.671-675, 2011 IEEE, World Congress on Information and Communication Technologies Dec. 11 -14, 2011

[5] Z. Abid, et. al., "PPM adder designs," in roceedings of IEEE CCECE, 2005, vol. 4, pp. 226 – 229, May 2005

[6] Ahmed M. Shams et al., "Performance Analysis of Low-Power 1-bit CMOS Full Adder cells," IEEE Trans. On VLSI systems, vol.10. No.1Feb, 2002.

[7] Guyot, Y. Herreros and J. Muller, "JANUS, an on-line multiplier/divider for manipulating large numbers," in Proceedings of 9th Symposium on Computer Arithmetic, pp. 106-111, 1989.

[8] H. R. Srinivas, K. K. Parhi and L. A. Montalvo, "Radix 2 Division with Over-Redundant Quotient Selection", IEEE Transactions on Computers, Vol. 46, No. 1, pp. 85-92, Jan. 1997

[9] Rizwan Mudassir, H. El-Razouk, Z. Abid and Wei Wang, "New designs of 14-transistor PPM adder." Canadian Conference on Electrical and Computer Engineering, pp. 1739-1742, May 2005

[10] M.A. Elgamel, S. Goel, and M.A. Bayoumi, "Noise tolerant low voltage XOR-XNOR for fast arithmetic," in Proc.Great Lake Symp. VLSI, Washington DC, Apr. 28-29,2003, pp. 285-288.

[11] S. Goel, M. E. Elgamel, M. A. Bayouni, and Y. Hanafy, "Design Methodologies for high- performance Noise-tolerant XOR-XNOR Circuits",IEEE Trans. Circuits and Syst. I, vol. 53, no. 4, April 2006.

[12] Goel, S.; Kumar, A.; Bayoumi, M. A., "Design of Robust, Energy-Efficient Full Adders for Deep-Sub-Micrometer Design Using Hybrid-CMOS Logic Style", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume:14, Issue:12 , pp. 1309 – 1321,2006.

[13] Shiv Shankar Mishra, Adarsh Kumar Agrawal, R.K. Nagaria, "A Comparative Performance Analysis of Various CMOS Design Techniques for XOR and XNOR Circuits", International Journal on Emergin Technologies, Vol.1, No.1 pp.1-10, Jan. 2010

[14] Ramracksha Tripathi, Shivshankar Mishra, "A Novel 14-Transistors Low-Power High-Speed PPM Adder", International Symposium on Electronic System Design,2011 IEEE DOI 10.1109/ISED.2011.19