Low-Power SRAM Cell at Deep Sub-Micron CMOS Technology for Multimedia Applications.

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***Abstract*— Our life is filled by various modern electronic products. Semiconductor memories are essential parts of these products and have been growing in performance and density in accordance with Moore's law like all silicon technology. The process technology has been scaling down from last two decades and to get the functional and high yielding design beyond 100-nm feature sizes the existing design approach needs to be modified to deal with the increased process variation interconnects processing difficulties, and other newly physical effects. Considerable increase in gate direct tunneling current in the nano-CMOS regime is because of scaling of gate oxide. Subthreshold leakage and gate direct tunneling current are no longer second-order effects. The effect of gate-induced drain leakage (GIDL) is easily visible designs, such as DRAM and low-power SRAM. All these effects cannot be ignored as it will lead to nonfunctional SRAM, DRAM, or any other circuit. Reducing the supply voltage which is now not a feasible solution in respect to stability of the SRAMs and on reducing the supply voltage the stability also disturbs. Power management is also a challenge in mobile applications. In this paper we have used leakage reduction technique to reduce the leakage power which reduces the leakage power from 40% to 50% for the SRAM cell at 45nm technology.**

Keywords—Tunneling current, GIDL, Feature Size, Process Variation

I. Introduction

The four major challenges for having low voltage leakage : reducing the leakage current, maintaining the signal voltage and signal charge of RAM cells, reducing the speed variations caused by variations in MOSFET threshold voltage , and reducing the cell size. Of these, the leakage current issue is especially important because leakage loses the low-power advantages of CMOS circuits that we take for granted today. There are two major types of leakage. The first is sub-threshold current and the second is gate-tunneling current in MOSFETs, both of which increase rapidly when Threshold voltage and the gate oxide thickness are reduced. Both types greatly affect the operation of RAM cells and peripheral circuits, not only in the standby mode but also in the active. As reducing sub-threshold current depends on circuit parameters while reducing gate tunneling current depends on process and device parameters. As the process technology continues to scale deeper into the nanometer region, the stability of embedded SRAM cells is a growing concern. The supply voltage must scale down accordingly to control the power consumption and maintain the device reliability. Scaling the supply voltage and minimum transistor dimensions that are used in SRAM cells challenge the process and design engineers to achieve reliable data storage in SRAM arrays.

In [4] the proposed 9T SRAM cell which has better stability. Stacking of PMOS has been used in this cell. The SRAM been simulated at 45nm 65% increase in SVNM compared to 6T SRAM cell. The cell has 33% leakage power reduction also with respect to 6T SRAM cell. So to reduce the further leakage power we used super cut off scheme which can further reduce the leakage power by 40%.

II. Working of SRAM Cell

In this section, cell is shown in Fig.1, as it is mentioned in [4], it is composed of two cross coupled P-P-N inverters, and data is stored in node Q and node Qb in a complementary manner. Transistors P1, P3, and N1 form a P-P-N inverter and P0, P2, N0 form another.

The source terminal of this transistor is connected to the RWL, which connects to the ground voltage only during the read operation. Otherwise, it stays high to control unnecessary leakage current.V1 and V2 are located between the two cascaded P-MOS transistors forming the P-P-N inverter. Q and Qb are the storage nodes. BL and BLB are bitlines while WL is the word line as in conventional 6T SRAM cell.

A. *Write Operation*

To perform a write operation, the wordline WL is enabled and one bitline, e.g., BLB, is pulled down to ground in advance. When the supply voltage is relatively high (e.g., 1 V), node Qb (storing '1') here in this case will be pulled down directly through the discharging path formed by. In turn, node Q will be charged up to complete the data-flipping process.

In general, the lower portion of our P-P-N inverter pair can be viewed as a latch consisting of P3-N1and P2-N0. In some sense, this latch takes node V1and node V2 as the pseudo supply terminals.

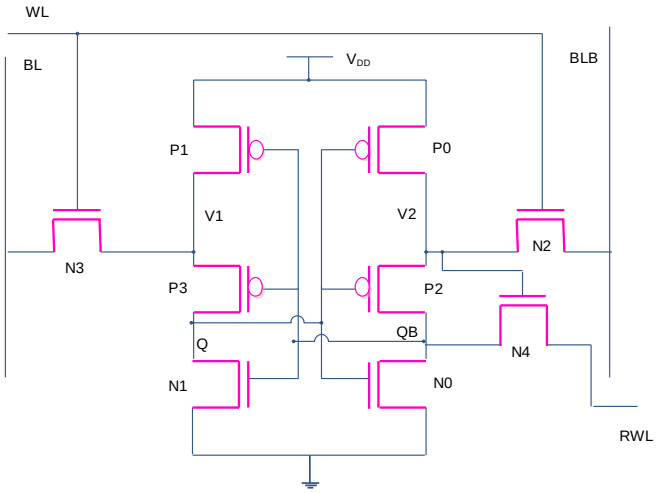

Fig.1. The P-P-N SRAM Bit-Cell

During this time period, P3 and P2 controlled by Qb still conducts weakly to pull up voltage at node Q, Due to the coupling effect of parasitic capacitances the voltage of Qb, which is in the floating state, rises with node Q but only slightly. In step 2, the data flipping finally takes place when Q is strong enough to conduct the transistor to discharge Qb down to the ground voltage.

B. *Read Operation*

To perform a read operation, the wordline WL is enabled and RWL is pulled down to ground to allow bitline discharging. shows the state of each transistor during the read operation, assuming that the data stored at Q is now '0'. Since data node Q and Qb are isolated from bitline BL by P2 and PP3 (which is between the true storage node Q) and thus the so-called read current (which is the current used to discharge a bitline) does not flow through the storage

III. Analysis of SRAM Cell

A. *Stability Analysis*

The stability of the cell is being calculated in terms of Static Noise Margin. The static noise margin (SNM) is the maximum amount of noise voltage that can be tolerated at the both inputs of the cross-coupled inverters in different directions while inverters still maintain bi-stable operating points and cell retains its data [1-2]. In other words, the static noise margin (SNM) quantifies the amount of noise voltage required at the storage nodes of SRAM to flip the cell data. The SNM is calculated at different process corners ie the five process corners (SS,TT,FF,FS,SF) at different voltages Vdd (0.5V -1.0V) as in Table-I. The temperature is taken 50^{o}C and all the simulation is done at 50^{o}C.The maximum SNM was at maximum voltage and at 1.0V the maximum SNM is at 374mV for TT corner. The highest SNM is 394mV.

Table-I SNM at different process corners

VDD	SNM(V) at different corners				
(V)	SS	TT	FF	SF	FS
0.5	0.184	0.174	0.174	0.154	0.154
0.6	0.224	0.224	0.214	0.204	0.195
0.7	0.274	0.264	0.254	0.244	0.244
0.8	0.314	0.304	0.284	0.284	0.284
0.9	0.354	0.344	0.314	0.324	0.324
1	0.394	0.374	0.344	0.364	0.354

B. *Leakage Analysis*

In this cell we have achieved 33% less leakage power with respect to 6T SRAM cell ,as in this cell we have used the PMOS cell and also we used ND3 which is used to reduce the leakage power. We have seen the effect of Vdd and temperature on leakage power. As we know it depends exponential to Temperature and increases with temperature the same affect is seen here in Fig.2

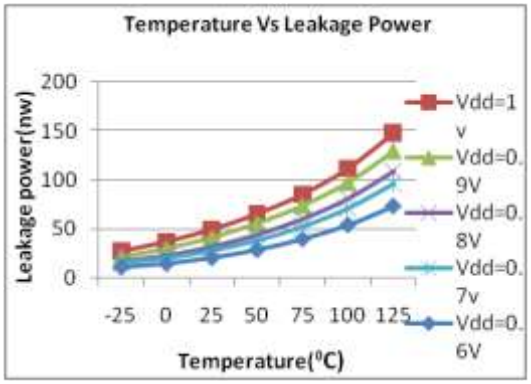

Fig.2 Temperature V/s leakage power

It also shows the effect of Vdd which shows that there is 7 times increases in Leakage power when we increase the Vdd from 0.6V to Vdd 1V.

IV. Leakage Reduction Technique

The subthreshold leakage current is exponentially dependent on the gate-to-source voltage of a MOSFET. Applying negative gate-to-source voltage (VGS) to an NMOS transistor suppresses the subthreshold leakage current. The Vgs (gate to source voltage) was kept at -25mv and the leakage power was change by upto 34%.When we further change the Vgs to -10mv and 0V the leakage power was reduced by 44% and 53% respectively. So we have applied this scheme in our proposed cell to reduce the leakage power. Leakage power at various Vgs is as shown in Table II .From

table II we can see that if we increases the Vgs beyong -50mv it will increase the leakage power drastically.

Table II. Leakage power using reduction technique

Vdd (V)	Leakage Power at various Vgs					
	0.0 mV	-10 mV	-25 mV	-50 mV	-75 mV	-100 mV
0.6V	5.023 pW	6.04 pW	7.03p W	11.6 pW	24.13 pW	56.07 pW
0.7V	7.051 pW	8.02p W	9.26 pW	15.0p W	30.68 pW	70.5p W
0.8V	8.98 pW	10.3 pW	11.8 pW	18.9 pW	37.97 pW	86.5 pW
0.9V	11.6 pW	13 pW	14.8 pW	23.2 pW	46.04 pW	104 pW
1.0V	14.65 pW	16.1 pW	18.2 pW	28.2 pW	54.97 pW	123 pW

In table III, the leakage power of PPN cell at various voltages without super cutoff is also been calculated and it can be clearly seen that Vgs 0V the leakage power is almost 50% to that of without using the leakage reduction technique. At 1 V without leakage reduction technique the power is again almost 50% of that using with reduction technique so we can say that the power is reduced by 50%, if we increases the Vgs beyond -50 mV it will increase leakage power.

Table III. Leakage power without reduction technique

Vdd/Vdata	Pstandby (pw)
0.6V	10.8 pW
0.7V	12.6 pW
0.8V	15.7 pW
0.9V	19.2 pW
1.0V	22.9 pW

CONCLUSION:

The cell has 33% leakage power reduction also with respect to 6T SRAM cell and in this we have not used any leakage reduction techniques. The static noise margin of the 9T SRAM cell in [5] was 300mv for 1.0V at 65nm and at 32 nm it was reported as 367mV at 0.9Vin [6] but for this it is 374mv at 1.0V in TT corner. The leakage current of the cell as in without using any leakage reduction technique was 75.8pw but after using super cut off scheme it has been drastically reduced to 14.65pw.So the cell is good choice for low power applications as well as where stability is a major concern.

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