Design and Simulation of High Level Low Power 7T SRAM Cell Using Various Process & Circuit Technique

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Abstract

Low power memory is required today most priority with also high stability. The power is most important factor for today technology so the power reduction for one cell is vital role in memory design techniques. In this paper we introduced some design circuit techniques for low power design. Leakage current in standby mode is the major part of power loss. We concentrate on the technique that to reduced the leakage current in standby mode.

Keywords: CMOS, SRAM, Threshold Voltage, Circuit techniques, Process Technique

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I. INTRODUCTION

Static random access memory (SRAM) is a type of volatile semiconductor memory to store binary logic '1' and '0' bits. SRAM uses bistable latching circuitry made of Transistors MOSFETS to store each bit. When the cell is selected, the value to be written is stored in the cross-coupled flip-flops. A basic SRAM cell consists of two cross coupled inverters forming a simple latch as storage elements and two switches connecting these two inverters to complementary bit lines to communicate with the outside of the cell shown in fig-1.

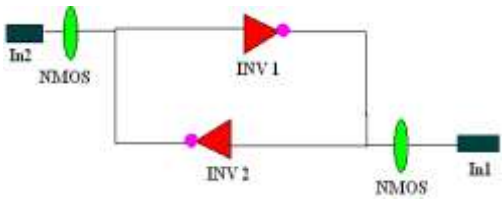

Fig-1

Cross-coupled inverters SRAM memory cell

The one CMOS transistor leakage current due to various parameter is the vital role of power consumption. The CMOS leakage current at the process level can be decreased by some implement on deep sub micron method. The circuit level technique is reduced power

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consumption at very high level. In this paper we simulate the 7T SRAM cell using many techniques both circuit level, process level in one cell as Hybrid cell.

II. THE 7T SRAM CELL

The circuit of 7T SRAM cell is made of two CMOS inverters that connected to cross coupled to each other with additional NMOS Transistor which connected to read line and having two pass NMOS transistors connected to bit lines and bit-lines bar respectively. Fig-2 shows circuit of 7T SRAM Cell, where the access transistors MN3 is connected to the word-line (WL) to perform the access write and MN4 is connected to the Read-line (R) to perform the read operations thought the column bit-lines (BL and BLB). Bit-lines act as I/O nodes carrying the data from SRAM cells to a sense amplifier during read operation, or from write in the memory cells during write operations. All transistors have minimum length (L_{MIN} =45nm according to used Technology), while their widths are typically design parameters. The value of W_{P1} and W_{P2} defines PMOS transistors width and W_{N1} and W_{N2} defines the NMOS driver transistors width use in CMOS Invertors,
while W_{N3} and W_{N4} is the access transistors width.

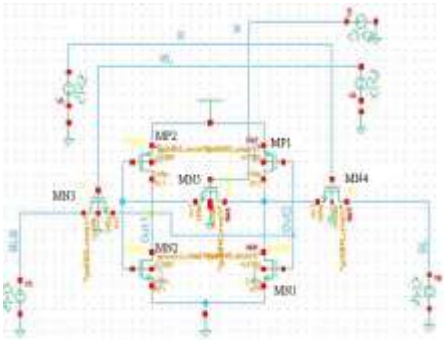

Fig-2 (a) Schematic

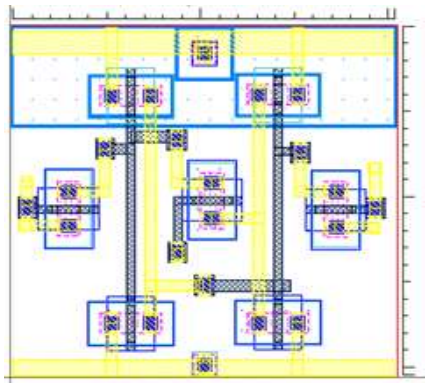

Fig-2 (b) Layout
Fig-2 Seven Transistor SRAM cell

III. CMOS LEAKAGE CURRENT

In the CMOS devices, the leakage current is becoming a major contributor to the total power consumption. In current deep-sub nanometer technology with low threshold voltages, sub threshold and gate leakage have become dominant sources of leakage and are expected to increase with the technology scaling. The leakage power is becoming significant component of the total power and may contribute to majority of the power dissipation in future *CMOS* technologies [1]. The leakage current and leakage power are increasing with scaling. The two main sources of power dissipation in CMOS circuits are dynamic power dissipation and static power dissipation. Static power dissipation is due to leakage current when the transistor is normally off. The improvement in technology scaling has introduced very large sub threshold leakage current, therefore careful

design techniques are very important in order to reduce sub threshold leakage current for low power design. Leakage current occurs in both active and standby modes. It is

recommended to switch off the leakage current when the circuit is in standby mode. The power and technology graph shown in fig-3.

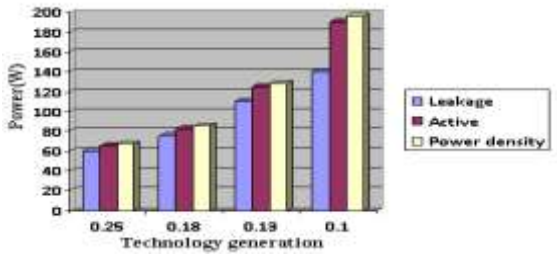

Fig-3. Static and dynamic power trends

There are Six main sources of leakage current in a CMOS transistor as shown in Fig-4.

1. Reverse-biased junction leakage current (I_{REV})
2. Sub threshold (weak inversion) leakage (I_{SUB})
3. Oxide tunneling Current (I_G)
4. Gate current due to hot-carrier injection
5. Gate induced drain leakage (*IGIDL*)
6. Channel punch through current

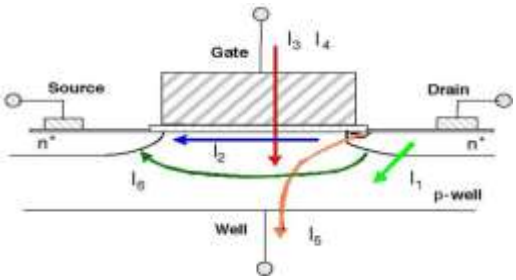

Fig-4 Leakage current mechanism in CMOS Transistor

A. Reverse-biased leakage current

Drain and source to well junctions are typically reverse biased, causing p-n junction leakage current. A reverse-bias p- n junction leakage (I_1) has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction [2]. For an MOS transistor, additional leakage can occur between the drain and well junction from gated diode device action (overlap of the gate to the drain-well pn junctions) or carrier generation in drain to well depletion regions with influence of the gate on these current components [3]. pn junction reverse-bias leakage (I_{REV}) is a function of junction area and doping concentration [4].

B. Sub threshold leakage (I_{SUB})

The Sub threshold is the drain-source current of a transistor operating in the weak inversion region. Unlike the strong inversion region in which the drift current dominates, the sub threshold conduction is due to the diffusion current of the minority carriers in the channel for a MOS device. In current CMOS technologies, the sub threshold leakage current, I_{SUB}, is much larger than the other leakage current components [5]. This is mainly because of the relatively low V_T in modern CMOS devices. I_{SUB} is calculated by using the equation (1)

$$I_{SUB} \quad {}_{th}{}^{2}C_{STH} \quad e^{\frac{Vgs-Vt+\eta Vds}{n\,Vth}} \quad .1$$

where *W* and *L* denote the transistor width and length, μ denotes the carrier mobility, V_{TH} = is the thermal voltage at temperature T, C_{STH} = Finally, complete content and organizational editing before formatting. Please take note of the following items when proofreading spelling and grammar:

C_{DEP}+ Cit denotes the summation of the depletion region capacitance and the interface trap capacitance both per unit area of the MOS gate , and η is the drain-induced barrier lowering (DIBL) coefficient [6] n is the slope shape factor and is calculated by equation-2

$$n = 1 + \quad \ldots\ldots\ldots\ldots\ldots\ldots \ldots \quad 2$$

C. Oxide tunneling Current (I_G)

Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from substrate to gate and also from gate to substrate through the gate oxide, resulting in the gate oxide tunneling current. Ignoring the effect of finite temperature and image-force-induced barrier lowering, the current density in the FN tunneling is given by equation-3

$$J_{FN} = \frac{q^3 E^2}{16\pi^2 h} \quad \ldots\ldots .3$$

Where E_{OX} is the field across the oxide; $Ø_{OX}$ is the barrier height for electrons in the conduction band; and m^* is the effective mass of an electron in the conduction band of silicon. The FN current equation represents the

tunneling through the triangular potential barrier and is valid for $V_{OX} > Ø_{OX}$, where is the voltage drop across the oxide

D. Gate current due to hot-carrier injection

In a short-channel transistor, due to high electric field near the Si–SiO_2 interface, electrons or holes can gain sufficient energy from the electric field to cross the interface potential barrier and enter into the oxide layer. The injection from Si to SiO_2 is more likely for electrons than holes, as electrons have a lower effective mass than that of holes and barrier height for holes (4.5ev) is more than that for electron

E. Gate induced drain leakage

GIDL is due to high field effect in the drain junction of an MOS transistor. When the gate is biased to form an accumulation layer at the silicon surface, the silicon surface under the gate has almost same potential as the p-type substrate. Due to presence of accumulated holes GIDL is due to high field effect in the drain junction of an MOS transistor. When the gate is biased to form an accumulation layer at the silicon surface, the silicon surface under the gate has almost same potential as the p-type substrate. Due to presence of accumulated holes

F. Channel punch through current Using the Template

In short-channel devices, due to the proximity of the drain and the source, the depletion regions at the drain-substrate and source-substrate junctions extend into the channel. As the channel length is reduced, if the doping is kept constant, the separation between the depletion region boundaries decreases. An increase in the reverse bias across the junctions (with increase in V_{DS}) also pushes the junctions nearer to each other.

IV. LEAKAGE REDUCTIONS AT PROCESS LEVEL

In an SRAM cell, the total power dissipation in dynamic and static components during the active mode. In the standby

mode, the power dissipation is due to the standby leakage current. Dynamic power dissipation consists of two components. One is the switching power due to charging and discharging of load capacitance. The other is short circuit power due to the nonzero rise and fall time of input waveforms. The static power of a CMOS circuit is determined by the leakage current through each transistor. The dynamic (switching) power (P_D) and leakage power (P_{LEAK}) are expressed as

$$P_D = \alpha f C V_{DD}^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 4$$

$$P_{LEAK} = I_{LEAK}. V_{DD} \quad \ldots\ldots\ldots\ldots\ldots\ldots 5$$

Where α is the switching activity; f is the operation frequency; C is the load capacitance. The substrate doping concentration should increase to decrease the depletion width proportionally. The principle of constant field scaling lies in scaling the device voltages and the device dimensions by the same factor, In addition to gate oxide thickness and junction scaling, another technique to improve short-channel characteristics is well engineering. By changing the doping profile in the channel region, the distribution of the electric field and potential contours can be changed. The goal is to optimize the channel profile to minimize the OFF-state leakage while maximizing the linear and saturated drive currents.

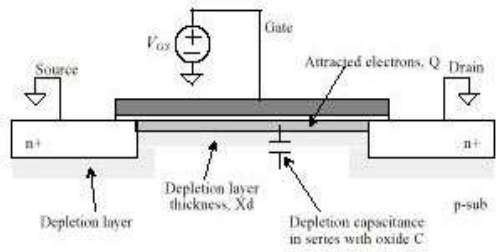

Fig-5 MOSFETs Graphical Representation

V. LEAKAGE REDUCTIONS AT CIRCUIT LEVEL

There are various techniques for leakage reduction at circuit level. To reduce the leakage currents, the use of higher . Transistor should be influenced through the bulk and DIBL coefficients. As these coefficients is only technology. For the gate leakage current only the voltages across the gate oxide can be adjusted. There are some methods.

A. Self Reverse Biasing

The body effect in CMOS transistors, a smaller width of the depletion layer leads to lower V_T. The reverse biasing of CMOS transistor increases V_T while on forward biasing of the COMS transistor V_T decreases. And also in CMOS threshold voltage increases with increased doping of the channel but decreases with applied bias. Therefore the current in the sub threshold region can be partially decreased by reverse biasing.

Equation (6) quantifies the back-gate bias parameter as function of the oxide capacitance and substrate doping level [7].

$$\ldots\ldots\ldots\ldots\ldots 6$$

Where is gate oxide thickness, is substrate doping level q is unity electron charge is gate oxide permittivity and is Silicon permittivity.

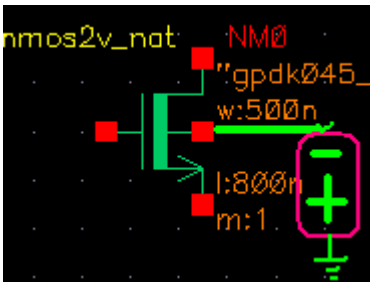

Fig 6 MOS Transistor With Reversed Biased

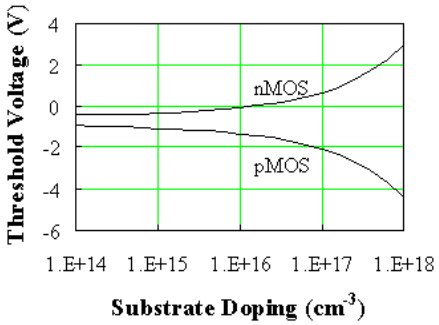

Fig-7 Threshold voltage of *n*-type (upper curve) and *p*-type (lower curve) MOSFETs versus substrate doping density

B. Multiple V_{TH} Designs

Multiple-threshold CMOS technologies is most popular and easy technique which put high V_T and low V_T transistors in a same chip, very effectively in leakage problem. The high-threshold transistors can partially decreased sub threshold leakage current, while the low-threshold transistors are used for high performance and Stability.

Multiple-threshold voltages can be achieved by the following methods.

1) Multiple channel doping

The threshold voltage equals the sum of the flat band voltage, twice the bulk potential and the voltage across the oxide due to the depletion layer charge.

$$V_T = V_{FB} + 2\varphi_F + \frac{\sqrt{2\,\epsilon_q\, qN_a(2\varphi_F + V_{SB}}}{C_{OX}}$$

Where the flat band voltage, V_{FB} is given by

$$V_{FB} = \varphi_{FB} - \frac{Q_F}{C_{OX}} - \frac{1}{C_{OX}} \int_0^{t_{OX}} \frac{x}{x_{OX}} \rho_{OX}(x)\, dx$$

With

$$\varphi_{MS} = \varphi_M - \varphi_S = \varphi_M - (x + \frac{E_g}{2q} + \varphi_F)$$

And

$$\varphi_F = V_t \ln \frac{N_a}{n_i}, p - substrate$$

And the similar for pMOS

$$\varphi_F = V_t \ln \frac{N_d}{n_i}, n - substrate$$

The threshold voltage dependence on the doping density is illustrated with for both *n*-type and *p*-type MOSFETs with an aluminum gate metal. The threshold of both types of devices is slightly negative at low doping densities and differs by 4

times the absolute value of the bulk potential. The threshold of nMOSFETs increases with doping while the threshold of pMOSFETs decreases with doping in the same way.

A variation of the flat band voltage due to oxide charge will cause a reduction of both threshold voltages if the charge is positive and an increase if the charge is negative.

2) Multiple Oxide CMOS (M_{OX})

Gate oxide thickness can be used to modify the threshold voltage of a transistor Dual can be achieved by depositing two different oxide thicknesses lower oxide thickness, and hence lower threshold voltage, in critical paths maintains the performance. Higher oxide thickness not only reduces the sub threshold leakage, it also reduces: a) gate oxide tunneling, since the oxide tunneling current exponentially decreases with an increase in the oxide thickness [8]; b) dynamic power consumption, since higher oxide thickness reduces the gate capacitance, which is beneficial for reduction of the dynamic power

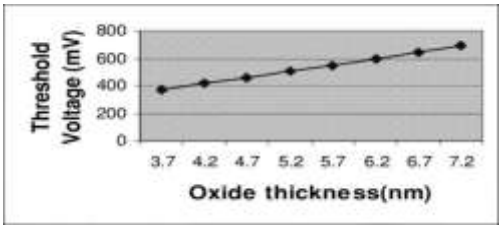

Fig-8 V_{TH} at different oxide thicknesses

*3) Multiple threshold voltage *

Employing transistors of both high and low values in a single chip along with a sleep control mechanism is the easiest method of reducing static power component. Use of higher transistors outside the critical path reduces static power consumption without compromising operational speed.

4) Multiple supply voltages

Applying different supply voltages is another way of reducing the leakage currents because the drain-source voltage of PMOS and NMOS transistors are closely linked to the supply voltage and power dissipation decreases quadratically with the scaling of supply voltage. Although the reduction of power supply voltage significantly reduces the dynamic power dissipation the inevitable design tradeoff is the increase of delay. Since the delay is proportional to it is possible to use high supply voltage in the critical paths of a design to achieve the required performance while the off critical paths of the design use lower supply voltage to achieve low power dissipation.

5) Dual Supply SRAMs

In CMOS SRAMs there are two important performance metrics, fast accessing speed and retention of the stored data. To fulfill this objective using two supplies to allow the SRAM to run in two different modes. A nominal supply voltage is used for powering of the peripheral circuits as decoders, sense-amplifiers and control circuitry and a secondary lower supply is used for idle cells. This effectively lowers the leakage currents of the idle cells. This idea can be utilized in many different ways. In [9] whole banks are put in a drowsy mode and require one or more clock cycles to be accessed. Resultant power saving are predicted in the order of 50% to 75%.

VI. . SIMULATION AND RESULT

We simulate various SRAM cell on cadence tool in different-different mode and technique and circuit parameter in 6T SRAM and 7T SRAM and found that 7T is the most prominent low power consumption cell. The fig-9 is shown hybrid 7T-SRAM cell with use various circuit technique and process. The leakage power is reduced by high level using various techniques. The fig-10 showed the leakage current and power with compare of 6T SRAM cell and 7T SRAM cell with also process and circuit level techniques modeling. Its also compare with hybrid model of 7T SRAM cell.

We have clear that V_T is the most appropriate parameter for reducing leakage power and current. By increasing doping and decreasing T_{OX} reduced power consumption.

The Equation-7 show that the threshold voltage dependent on various parameters on SRAM cell. Here we can see that the threshold can changed by Ø, γ and η. They are easily change by well engineering design.

$$V_T = V_{TO} + \gamma(\sqrt{(-2\emptyset f)} - 1 \quad \ldots\ldots 7$$

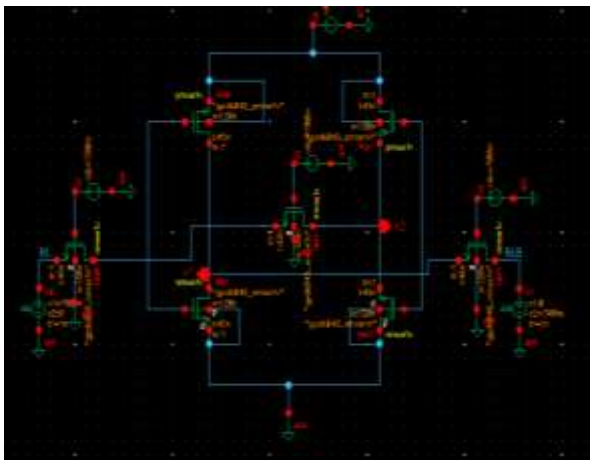

Fig-9 Used High Level circuit and process technique Simulated 7T SRAM

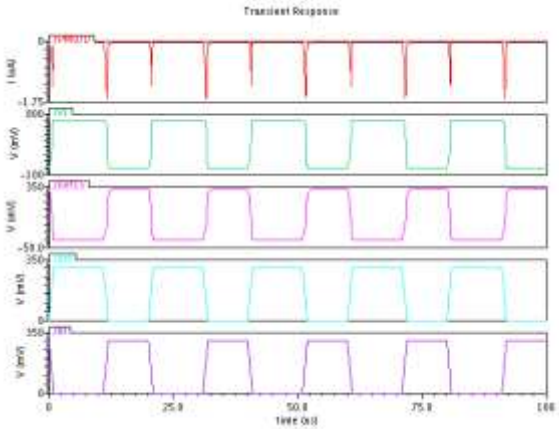

Fig-10 Leakage current for 7T SRAM

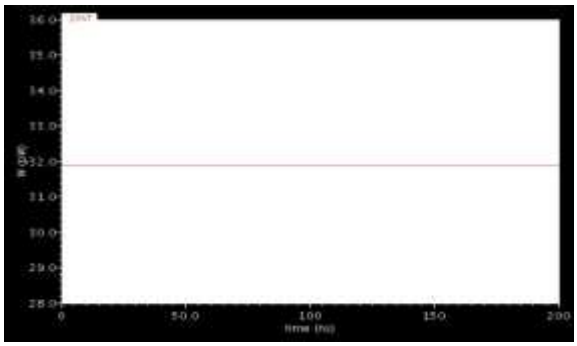

Fig-11 Leakage power for 7T SRAM

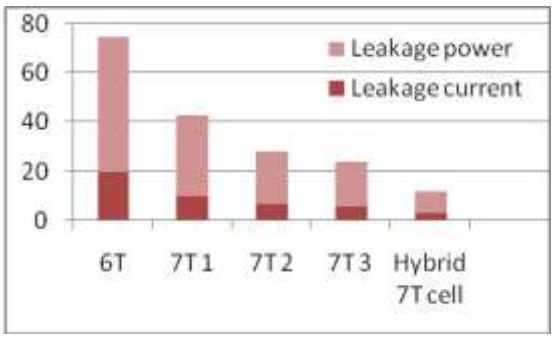

Fig 12- Various result of current and power

ACKNOWLEDGEMENT

I am very thankfully to H.I.T.M for providing a good lab facility. We simulate the Result on ***CADENCE VIRTUOSO Tool***.

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