Analysis and Simulation of a Low-Leakage 10T SRAM Bit-Cell using Dual-V_{th} Scheme at Deep Sub-Micron CMOS Technology

R.K.Singh[1], Manisha Pattanaik[2], Neeraj Kr. Shukla[3], S.Birla[4], Sveen Nagpal[5]
[1]BCT-Kumaon Engineering College, Dwarahat, Almora, (Uttarakhand), India
[2]ABV-Indian Institute of Information Technology & Management, Gwalior, (Madhya Pradesh), India
[4]Sir Padampat Singhania University, Bhatewar, Udaipur (Rajasthan), India
[3,5]ITM University, Gurgaon, (Haryana), India

***Abstract*— Exponential growth of battery powered portable applications demanding new SRAM cell topologies with low-leakage. In this work, an analysis and simulation on P-P-N based 10T SRAM cell using dual-V_{th} scheme (at deep sub-micron technology) is presented. This work achieved stand-by leakage reduced by 74% and 77% at VDD=0.8V and VDD=0.7V respectively without losing cells performance at an area power trade-off. The simulation is being performed at 45nm CMOS technology, V_{thn}=0.22V, V_{thp}=0.224V, V_{DD}=0.7 and 0.8V, and at T=27^{0}C.**

***Keywords*— Low power SRAM, Schmitt trigger, deep sub micron, Dual-Vth**

I. INTRODUCTION

With the dependence of the leakage power on the number of transistors, and given the projected large memory content of future SoC (System on Chip) devices (more than 90% of the die area by 2014 [1]), it is important to focus on minimizing the leakage power of SRAM structures**.** As the CMOS process technology continues to scale to the nanometer regime, process variation and leakage current of transistors become more severe, which are further aggravated by the fluctuation of the operation conditions such as the variation of the supply voltage and/or the temperature leads to a higher chance of device malfunctioning. Furthermore, leakage is the only source of energy consumption in an idle circuit.

Hence, the design of low-leakage SRAM cell is highly desirable. The paper is organized as follows, Section II presents a brief functional overview of the Conventional 6T SRAM Cell, Section III explains briefly the P-P-N based 10T SRAM cell, Section IV gives the review of the related work that has been done in this area, whereas Section V gives the simulation work performed on dual-V_{th} 10T SRAM cell followed by the Conclusion in Section VI.

II. THE CONVENTIONAL 6T SRAM BIT-CELL – A FUNCTIONAL APPROACH

The Conventional SRAM (CV-SRAM) cell has Six MOS transistors (‘4’ nMOS and ‘2’ pMOS), Figure1. Unlike DRAM it doesn’t need to be refreshed as the bit is latched in. It can operate at lower supply voltages and has large noise immunity. However, the six transistors of an SRAM cell take more space than a DRAM cell made of one transistor and one capacitor thereby increasing the complexity of the cell [2].

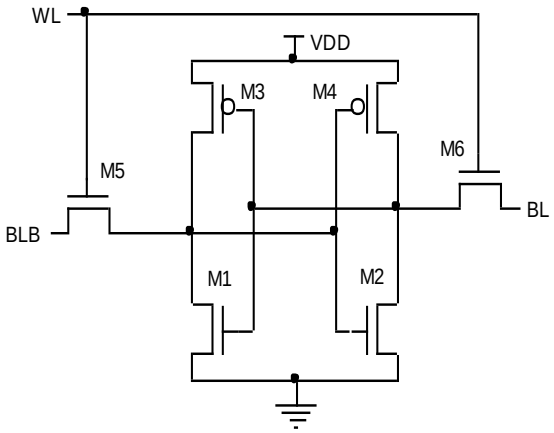

Figure 1 6T-CMOS SRAM Bit-Cell

A. *The SRAM Bit Cell*

The memory bit-cell has two CMOS inverters connected back to back (M1, M3, and M2, M4). Two more pass transistors (M5 and M6) are the access transistors controlled by the Word Line (WL), Figure 1. The cell preserves its one of two possible states ‘0’ or ‘1’, as long as power is available to the bit-cell. Here, Static power dissipation is small. Thus the cell draws current from the power supply only during switching. But ideal mode of the memory is becoming the main concern in the deep-sub-micron technology due to its concerns in the leakage power and data retention at lower operating voltages.

B. *The Operation of SRAM Bit-Cell*

Although the two nMOS and pMOS transistors of SRAM memory bit-cell form a bi-stable latch, there are mainly the

following three states of SRAM memory cell, the Write, Read, and Hold states.

1) Standby Operation (Hold): When WL = '0', M5 and M6 disconnect the cell from Bit-Lines (BL and BLB). The two cross-coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are disconnected from the outside world. The current drawn in this state from the power supply is termed as standby current.

2) Data Read Operation: Read cycle starts with pre-charging BL and BLB to '1', i.e., V_{DD}. Within the memory cell M1 and M4 are ON. Asserting the word line, turns ON the M5 and M6 and the values of Q and Q' are transferred to Bit-Lines (BL and BLB). The M4 and M6 pull BL upto V_{DD}, i.e., BL = '1' and BLB discharges through M1 and M5. This voltage difference is sensed and amplified to logic levels by sense amplifiers.

3) Data Write Operation: The value to be written is applied to the Bit lines. Thus to write data '0', we assert BL=0, BLB = '1' and to write data '1', the BL = '1', BLB = '0', asserted when WL = '1'.

III. The P-P-N Based 10T SRAM Cell

A 10T SRAM cell, Figure2, as the name suggests, consists of 10 transistors. Out of these transistors, four are pull-up transistors (PUL1, PUL2, PUR1 and PUR2), four are pull-down transistors (PDL1, PDL2, PDR1 and PDR2) and two are access transistors (PGL and PGR)[3]. The two pull-down transistors i.e. PDL1 and PDR1 are connected to VGND. This VGND signal is connected to ground during the read operation and VDD, otherwise. In 10T SRAM cell, the access transistors are connected to pseudo nodes (pQ and pQb i.e. nodes between two pull-up transistors) rather than the storage nodes (i.e. Q and Qb). Due to this, the storage nodes are isolated from the BLs and therefore during the read operation, the read current does not flow through the storage nodes and hence maintain the read stability. In case of the write operation, the VGND is connected to VDD and one of the bit-lines e.g. BL is grounded. Suppose the node Q is storing '1' and node Qb is storing '0'. When a high supply voltage is provided, the node Q is pulled down to '0' due to discharging through the access and the pull-up transistor i.e. PGL and PUL2.

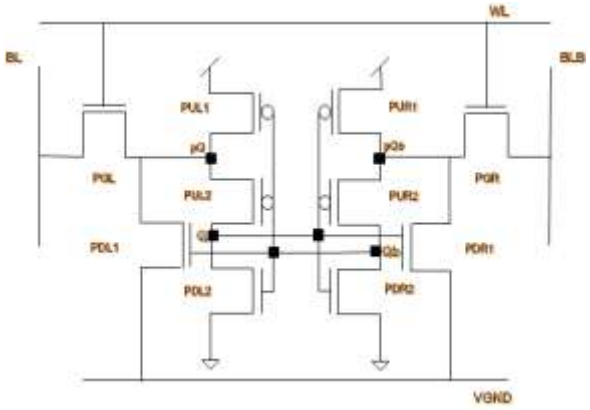

Figure 2. The 10T SRAM Cell

In this paper we have proposed a 10T SRAM cell using dual-Vth scheme. Here, we use standard Vth pull-up transistors, low Vth access transistors and high Vth pull-down transistors. Due to the low Vth transistors, the gate voltage (Vg) required for activation of the access transistors is low and thus, the access speed for the data stored increases considerably. Also the high Vth Pull-down transistors decrease the leakage in the circuit.

IV. A Review of Related Work

For the 6T SRAM, the cell stability and the write ability may sporadically experience data-flipping (i.e., a bit cell changes its state from '0' to '1' or *vice versa* after being read) or write failure (i.e., the data to be written into a bit cell fails to overwrite its previously stored value). To cope with these problems, several new SRAM cells equipped with some supportive peripheral circuits have been proposed like the single-ended sensing cells [4]–[8] and differential sensing cells [9], [10]. In general, a single-ended sensing cell is not as robust as the differential one, and hence, it often requires some extra compensation scheme to maintain the reliability as proposed in [7]. Moreover, it is not easy if not impossible for a single-ended sensing cell to support column multiplexing (also known as *bit-interleaving*) in which an IO is shared among several cell columns. In the differential cells, the stability and writeability of the cell have been improved by using two cross-coupled Schmitt-trigger inverters to form the storage cell. There is a minor problem with this type of *ST cell* – it still suffers from the *read disturbance problem*, which refers to the phenomenon that a storage node with data '0' will experience a *transient voltage glitch* when it is being read. This voltage glitch may sometimes cause the cell to flip unexpectedly.

V. Simulation Work

In our work, we have used dual V_{th} scheme in 10T SRAM cell. The working of this cell is the same as the standard V_{th} 10T SRAM cell except for the access transistors (PGL and PGR), which are used here, have low V_{th} and the pull-down transistors (PDL2 and PDR2) have high V_{th}. As explained earlier, due to the low V_{th} of the access transistors, the access speed of the transistors increases considerably. This helps in faster access of the data stored in the SRAM cell. Also due to the high V_{th} pull-down transistors, the leakage of the circuit through theses transistors decreases. Hence, the performance of the cell increases as compared to the dual V_{th} 6T SRAM cell on an area-power trade-off.

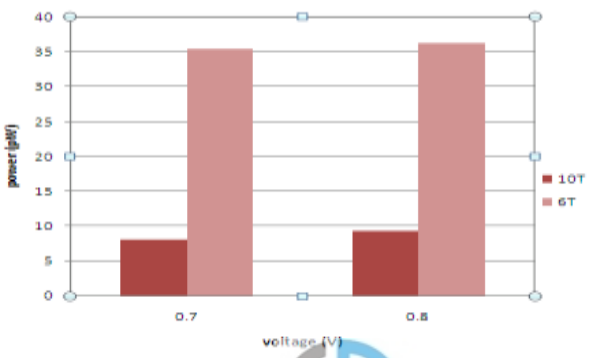

Figure 3. A comparison of Leakage Power of conventional 6T and 10T SRAM Cells

Figure 3 shows the static power dissipation of the dual-V_{th} 6T SRAM cell and the dual V_{th} 10T cell. As can be seen from the figure, the leakage power in dual-Vth 10T SRAM cell decreases by 74% and 77% as compared to the dual V_{th} 6T SRAM cell at V_{DD}=0.8V and 0.7V respectively, at room temperature.

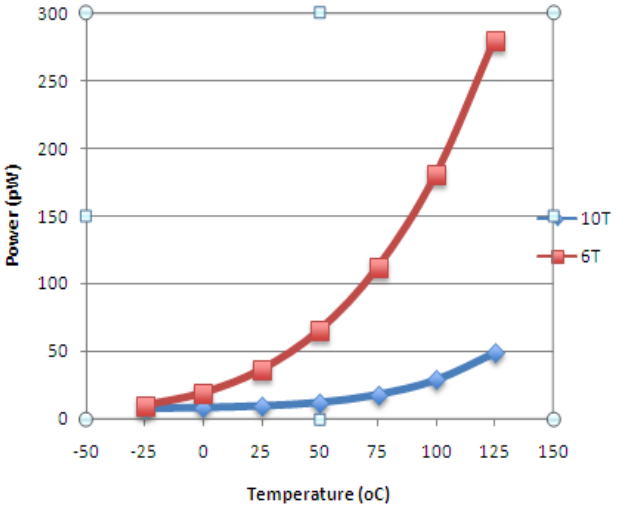

Figure 4. Effect of Temperature variations on conventional 6T and 10T SRAM Cell

Figure 4 shows the temperature variation of the dual Vth 6T and 10T SRAM cell over the temperature range –25 to 125 °C at 0.8V. In the dual Vth 10T SRAM cell, the leakage power decreases by 57%, 74%, 81% and 82 % at 0°C, 25°C, 50°C and 125°C, respectively as compared to dual-Vth 6T SRAM bit-cell.

Apart from the reduction in the stand-by leakage, the cell has shown considerably good amount of SNM i.e. 0.42V at VDD=0.8V and 0.37V at VDD=0.7V. Thus, the only parameter where the cell compromise, is its area as it uses 10 transistors instead of 6.

VI. Conclusions

In this paper, an analysis and simulation on P-P-N based 10T SRAM cell using dual-V_{th} scheme (at deep sub-micron technology) is presented. This work achieved stand-by leakage reduced by 74% and 77% as compared to dual-Vth 6T SRAM bit-cell at V_{DD}=0.8V and V_{DD}=0.7V, respectively without losing cells performance at an area power-tradeoff.

Acknowledgement

The authors are highly grateful to their respective organizations for their help and support..

References

[1] J. Abraham, “Overcoming timing, power bottlenecks,” EE Times, April 2003.

[2] Neeraj Kr. Shukla, R.K.Singh, Manisha Pattanaik, “A Novel Approach to Reduce the Gate and Sub-threshold Leakage in a Conventional SRAM Bit-Cell Structure at Deep-Sub Micron CMOS Technology”, International Journal of Computer Applications, Volume 23– No.7, June 2011, pp. 23-28.

[3] Cheng-Hung Lo and Shi-Yu Huang,“P-P-N Based 10T SRAM Cell for Low-Leakage and Resilient Subthreshold Operation”. , IEEE journal of solid-state circuits, VOL. 46, NO. 3, MARCH 2011

[4] B. H. Calhoun and A. Chandrakasan, “A 256 kb subthreshold SRAM in 65 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 680–688, Mar. 2007.

[5] T. Kim, J. Liu, J. Keane, and C. Kim, “A 0.2 V, 480 kb subthreshold SRAM with 1 k cells per bitline for ultra-low-voltage computing,” *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 518–529, Feb. 2008.

[6] B. Zhai, D. Blaauw, and D. Sylvester, “A variation-tolerant sub-200mV 6-T subthreshold SRAM,” *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2338–2348, Oct. 2008.

[7] N. Verma and A. Chandrakasan, “A 256 kb 65 nm 8T sub-Vt SRAM employing sense-amplifier redundancy,” *IEEE J. Solid-State Circuits*, Vol. 43, no. 1, pp. 141–149, Jan. 2008.

[8] T. Kim, J. Liu, and C. Kim, “A voltage scalable 0.26V, 64 kb 8TSRAM with Vmin lowering techniques and deep sleep mode,” *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1785–1795, Jun. 2009.

[9] J. Kulkarni, K. Kim, and K. Roy, “A 160 mV robust Schmitt trigger based subthreshold SRAM,” *IEEE J. Solid-State* Circuits, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.

[10] I. J. Chang, J. Kim, S. P. Park, and K. Roy, “A 32 kb 10T subthreshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS,” IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 650–658, Feb. 2009.

ABOUT THE AUTHORS

R.K. Singh (IAENG, ACEEE, IE, ISTE), Professor in the Department of Electronics & Communication Engineering, Bipin Tripathi Kumaon Institute of Technology, Dwarahat, Almora (UK) India. He is being honored with the Ph.D. in Electronics Engineering in the Year 2003 from the University of Allahabad, Allahabad (Uttar Pradesh), India. He has received his M.E. (Electronics & Control Engineering) in 1992 from BITS, Pilani, (Rajasthan) India. He has around thirty five research publications in the conferences and journals at national and international repute. He has also guided eight ME thesis. He has authored seven text-books in the field of VLSI Design, Basic Electronics, and Opto-Electronics. He has worked at various capacities in the Academic domain such as, the Principal, Kumaon Engineering College, Dwarahat (Almora) Uttarakhand, India, in the year 2003-04, Director (O), Directorate of Technical Education, Uttaranchal in the year 2005, and Joint Director, State Project Facilitation Unit, Dehradun for the World Bank TEQIP Project. Apart from his industrial experience, he has contributed as a Scientist and Senior Scientist in Engineering Research at Central Electronics Engineering Research Institute (CEERI), Dehradun (UK) India, with a focus in Fibre Optics Communication and their subsequent application in optical devices to various other technologies and VLSI Design and Con Controls (P) Ltd. He is also the recipient of couple of prestigious awards, e.g., Rastriya Samman Puruskar, Jewel of India Award, Rastriya Ekta Award, Life Time Achievement Award, and Arch of Excellence Award. His current areas of interest are VLSI Design, Opto-Electronics and its applications.

Manisha Pattanaik (IEEE, IEICE, IE, ISTE), she has received the M.E. degree in Electronics Systems and Communication from National Institute of Technology, Rourkela, India in 1997. She received the Ph.D. degree in Electronics and Electrical Communication Engineering from the Indian Institute of Technology, Kharagpur, India in 2005. In 2007, she joined the Information and Communication Technology Faculty at ABV-Indian Institute of Information Technology and Management, Gwalior, India and is currently an Associate Professor. She has authored and coauthored over 40 papers in journals and conference proceedings in various areas of VLSI design. Her research interests include leakage power reduction of Nano-scale CMOS circuits, low power and low voltage static and dynamic logic circuit techniques for high performance

digital and analog VLSI applications, low power SRAM circuits, and CAD of analog and mixed signal integrated circuits.

Neeraj Kr. Shukla (IEEE, IACSIT, IAENG, IETE, IE, CSI, ISTE, VSI-India, UACEE), a Ph.D. Scholar at the UK Technical University, Dehradun (UK) India and an Asst. Professor in the Department of Electrical, Electronics & Communication Engineering, ITM University, Gurgaon, (Haryana) India. He has received his M.Tech. (Electronics Engineering) and B.Tech. (Electronics & Telecommunication Engineering) Degrees from the J.K. Institute of Applied Physics & Technology, University of Allahabad, Allahabad (Uttar Pradesh) India in the year of 1998 and 2000, respectively. His main research interests are in Low-Power Digital VLSI Design and its Multimedia Applications, Digital Hardware Design, Open Source EDA, Scripting and their role in VLSI Design, and RTL Design.

Shilpi Birla (IACSIT, IAENG), a Ph.D. Scholar at the UK Technical University, Dehradun (Uttarakhand) India is an Asst. Professor in the Department of Electronics & Communication Engineering, Sir Padampat Singhania University, Udaipur (Rajasthan) India. She has received her M.Tech. (VLSI Design) and B.E. (Electronics & Communication Engineering) Degrees from the University of Rajasthan, Jaipur (Rajasthan) India and MITS University, Laxmangarh, (Rajasthan) India, respectively. Her main research interests are in Low-Power VLSI Design and its Multimedia Applications, RF-SiP, and Low-Power CMOS Circuit Design.

Sveen Nagpal (UACEE) is a student of B.Tech. Final Year "Electronics & Communication Engineering" at ITM University, Gurgaon. Her research interests are Digital VLSI Design, Volatile Memory, Linux and Scripting.