Programmable PLL Based Digital Frequency Synthesizer-A Prototype Experiment

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Abstract— Frequency synthesizers are extensively used in radio, television and other wireless communication systems, whose performance will directly affect the overall performance of the system, particularly on the quality of transceivers. Many communication devices have digital frequency synthesizers that will provide a means for selecting a particular frequency or sweep through a frequency range using computer control or pushing button. A PLL based digital frequency synthesizer and it's operation is introduced in the paper firstly. Then introduced a CMOS PLL using MC145106 along with VCO 565 and a programmable divided by N-counter. Finally a prototype experiment is performed by designing sub circuits like loop filter, buffers and voltage shifters to improve the overall performance of the Frequency Synthesizer.

Index Terms—Frequency synthesizer, CMOS PLL, VCO 565, MC 145106 programmable divided by N counter.

I. INTRODUCTION

Not long ago, frequency synthesis was considered a novelty. Now, frequency synthesis is so natural that every radio design uses only synthesized signals for generation and control of signals. There is an increase in demand for frequency stability, spectral density and generation of one or more frequencies from a single source with the growth in the technology. Usage of PLL is one the best methods for improving the performance of Frequency synthesizer. [1][2]

The applications of PLL frequency synthesizer brought an increase in demand for configurable, wide-band and multi-frequency output PLL frequency synthesizer. Programmable divider is one of the key parts of Frequency synthesizer. It implements frequency de-multiplication of the input signal through software programming by using ATmega16 microcontroller.[3]

II.BASIC FUNCTIONAL BLOCKS IN A PLL

The PLL is an optimum phase estimator which include three basic components a phase detector (PD), loop filter (LP) and a voltage controlled oscillator (VCO). A feedback branch in which a frequency divider (N-counter) is inserted to form a single loop PLL as shown in Fig1.[4]

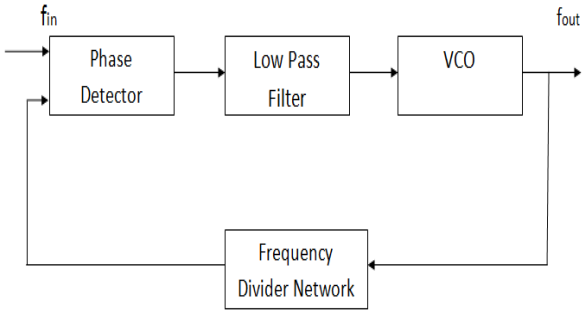

Fig.1 Block diagram of pll based frequency synthesizer

A. Phase detector: PD is an important functional block that compares the phase of the input signal f_{in} with the output phase of the VCO. The output f_{out} of the PD is proportional to the phase difference of two input signals. Phase detector is characterized by

$$V_{PFD} = K_{PD}\ \Delta\Phi \qquad (1)$$

Where the phase difference is given by

$$\Delta\Phi = \Phi_{in} - \Phi d_{div} \qquad (2)$$

Where K_{PD} is the phase detector gain.
Φ_{in} = phase of the reference signal
Φd_{div} = phase of divider by N counter.

B.Loop Filter: Loop filter plays a vital role in PLL, which can filter out high frequency components and noise in current or voltage form and transform them to error voltage components for guaranteed performance and loop stability.

C.Voltage Controlled Oscillator: As a frequency control devices of VCO acts as transducers (voltage in frequency), whose transfer characteristic is given as

$$F_{VCO}(t) = K_{VCO}\ V_{ctrl} \qquad (3)$$

When $\mathbf{V_{ctrl}}$ as the input control voltage of the VCO and K_{VCO} is VCO's gain.[5][6]

III. PROTOTYPE EXPERIMENT

A.Features and functions of MC 145106 chip: The MC 145106 is not a complete digital PLL, but it provides the divide-by-N digital input network, a crystal controlled reference clock frequency, and a digital phase detector. The reminder of the PLL is external to the MC 145106,figure 2 shows the circuit to be used in the experiment.[7]

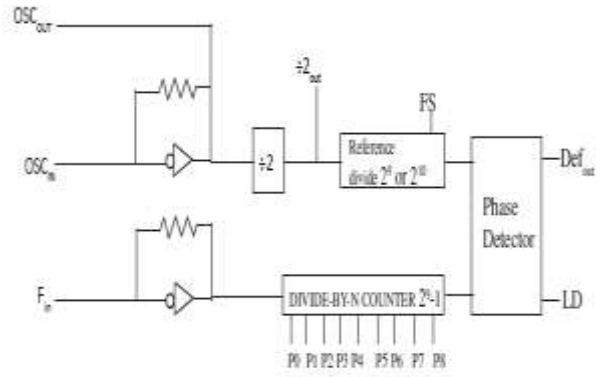

Fig.2 Internal block diagram of MC145106

B.MC145106operation: The internal operation of the MC145106 is depicted in the block diagram form in the figure 3. The chip contains three fundamental parts.

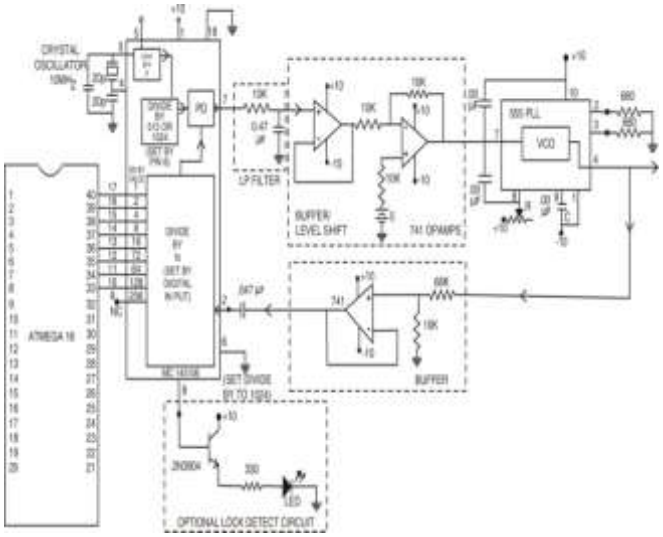

Fig 3.programmable PLL based frequency synthesizer MC145106

The circuitry to divide the crystal frequency by 2 and then again by 512 or 1024. The crystal frequency is divided by a total of 1024 or 2048. The selection of divide-by-1024 or divide by-2048 is made by opening (1024) or grounding (2048) pin 6.

The digital divide-by circuitry that takes the feed back signal at pin 2 and divides it by any number from 1 to 511 (there are 9 input pins, and 2^9=512).

The digital phase detector that compares the crystal frequency divided by 2048 with incoming frequency at pin 2 (divided by N), set by the digital input. The output of the phase detector is a pulse width modulated signal with a d.c. value proportional to the difference in frequency between the input signal (divided by N) and the crystal frequency (divided by 2048). The output of the phase detector is high when the input frequency is lower than the reference frequency and the low when the input frequency is higher than the reference frequency.

C.Circuit operation: The MC 145106 is used to control a VCO in a standard PLL configuration. The MC 145106 adds as the phase detector, and the crystal controlled input frequency adds as an input signal to the phase detector. The VCO output signal after division by N in the MC 145106 is compared with the crystal input frequency which is calculated as follows.

$$\text{Phase detector crystal input} = \frac{10\times10^6}{2048} = 4.883\,KH_Z$$

The 565 PLL is used as a convenient way of using an easily constructed VCO. The PLL loop is open in 565, so only the VCO portion of the 565 is being used. The low pass filter at the output of the MC 145106 phase detector (pin 7) converts the PWM output signal into a 0 to 10V signal (or close enough to d.c to control the VCO).

The two 741 OP AMPs between the low pass filter and the 565 provide a buffer and a level shifter to change the 0-10V signal to a signal compatible with controlling the 565 VCO frequency. The buffer between the 565 VCO the input of MC 145106 changes the amplitude of the signal to the level approximately 1V peak to peak that the MC145106 is capable of accepting.

D.Circuit calculations: The VCO is initially adjusted to a free running frequency of 100 KHz. To initiate the operation of overall PLL, set the divided – by-N inputs to the MC 145106 to a value that will make the input to the phase detector from the divided by –N circuit the same as input from the crystal is 4.883 KHz. Thus the other input of phase detector is also to be 4883 KHz.

$$\frac{Frequency\ of\ VCO(pin\ 4)}{Divide-by-N\ value} = 4882.8125$$

Since the divided by –N is in increments of 1, so N=21 initially.

This will provide a calculated frequency of 4882.8125 x 21 = 102539.0625 i.e 102.54KHz.

The limits on the band width of this VCO under these conditions are about 40 to 275 KHz. The lower limit on

$$N = \frac{40 \times 10^3}{4.8828 \times 10^3} = 8.192 \cong 9$$

Upper limit on

$$N = \frac{245 \times 10^3}{4.8828 \times 10^3} = 8.192 \cong 57$$

Therefore the range on N = 9 to 57

E.Final result: The free running frequency of VCO is 100 KHz whose N value is 21.
The lower limit of bandwidth is 43945.3125 Hz $\cong$ 43.95 KHz whose N value is 9.

The upper limit bandwidth is 278320.3125 Hz $\cong$ 278.32 KHz whose N value is 57.

F.ATmega16: ATmega 16 is an 8 bit high performance programmable micro controller of ATmega's Mega AVR family, with lower power consumption. Most of the instructions execute in one machine cycle. ATmega 16 can work on a maximum frequency of 16 Mhz. ATmera 16 is a 40 pin micro controller. There are 32 I/0 lines which are divided into four 8-bit ports designated as Port A, Port B, Port C and Port D.

Fig.3 for a frequency synthesizer including VCO output frequency through the buffer, loop pass filter whose output to the programmable PLL MC 145106 line input by the ATmega micro controller I/O port on MC 145106 be programmed to change its initial count of the counter, there by changing the frequency division ratio, dual output phase detector inputs error signal ϕ_V and ϕ_R to the loop pass filter and the smooth error voltage is directly controlled the voltage control oscillator VCO forming a complete phase locked loop frequency synthesizer

Table 1:

VCO (controlled voltage)	Theoretical Frequency	Measured Frequency
0	43.9453 KHz	47.6211 KHz
1	45.8725 KHz	49.9453 KHz
2	47.9211 KHz	52.5421 KHz
3	52.6392 KHz	56.4874 KHz
4	53.5281 KHz	57.3792 KHz

The above Table 1 shows that the output of VCO changes with its control voltage from phase detector by changing the N value in frequency divider divided by N-counter controlled by the Atmega 16 microcontroller. This shows that the prototype experiment is successful.

IV CONCLUSIONS

Wide range of frequencies has been generated by the designed experiment for usage. Understanding the theory and operation of digital frequency synthesizer as a simple versatile, good reliable a prototype experiment has been done.

Introducing programmable counter is a flexible, convenient and cost effective method, with strong practicality. Connecting phase locked loop frequency synthesizer to the corresponding pre scalar is easy to integrate and promote. Loop filter, and voltage control oscillator circuit will form the frequency synthesizer. The frequency synthesizer is with low phase noise, high frequency stability. Using of assembly language programming control sub frequency of MC 145106 chip through ATmega16 micro controller emulation, to achieve the right control of VCO's control voltage.

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