UACEE International Journal of Advances in Electronics Engineering Volume 2: Issue 3
ISSN 2278 - 215X (Online)

Analysis of Pseudo-NMOS Logic with Reduced Static Power in Deep Sub-Micron Regime

M. Janaki Rani
Research Scholar, ECE Dept.,
Sathyabama University,
Chennai, India
janakiranimathi@gmail.com

Dr. S. Malarkkan
Principal,
Manakula Vinayagar Institute of Technology,
Puducherry, India
malarkkan_s@yahoomail.com

***Abstract*- The growing demand for high density VLSI circuits result in scaling of supply voltage and an exponential increase of leakage or static power in deep sub-micron technology. Therefore reducing static power consumption of portable devices such as cell phones and laptop computers is highly desirable for a longer battery life. In this paper we propose two power reduction techniques such as reverse body bias and transistor stacking for reducing the static power of Pseudo NMOS logic circuits that have very high static power consumption. The simulation results show that the static power decreases with both the methods and the combined effect of reverse body bias and stack method gives the least static current. The simulations are done at 65nm and 45nm process technologies using HSPICE at a temperature of 27C with two different supply voltages of 1v and 0.3v.**

***Keywords*- Pseudo-NMOS logic, process technology, reverse body bias, transistor stack, static power.**

I. Introduction

Power has become one of the primary constraints for both the high performance and portable system design. Increasing demand for portable equipments such as cellular phones, personal digital assistants and notebook computers requires low power VLSI circuits for longer battery life [1]. With continuous technology scaling and increase in the number of transistors in a chip, the power consumption of the ICs increases. This higher power consumption raises the temperature of the ICs and directly affects battery life in portable devices. The increase in temperature results in increased cooling cost and complicated packaging techniques [2]. A significant portion of the total power consumption in high performance digital circuits is due to static or leakage currents. Leakage power makes up to 50% of the total power consumption in today's high performance microprocessors [3]. Therefore static or leakage power reduction becomes the key to a low power design. The leakage or static power dissipation is the power dissipated by the circuit when it is in standby mode and is given by (1).

$$P_{static} = I_{leak} * Vdd \quad (1)$$

Where I_{leak} is the leakage current that flows in a transistor when it is in OFF state and Vdd is the supply voltage. The leakage current consists of various components, such as sub-threshold leakage, gate leakage, reverse-biased junction leakage, gate-induced drain leakage [4]. Among these, sub-threshold leakage and gate-leakage are dominant. The sub-threshold leakage current of a MOS device can be modeled by (2) & (3).

$$I_{sub}=I_0 \exp [(V_{gs}-V_t) /(n V_T)] [1- \exp (-V_{ds}/V_T)] \quad (2)$$

$$\text{and } I_0=\mu_{eff} C_{ox} (W/L) V_T^2 \quad (3)$$

Where μ_{eff} is the electron/hole mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are width and length of the channel respectively, Vt is the threshold voltage, n is the sub-threshold swing co-efficient, V_T is the thermal voltage, V_{gs} is the transistor gate to source voltage and V_{ds} is the drain to source voltage.

The rest of the paper is organized as follows. Section II describes pseudo-NMOs logic and section III gives the proposed static power reduction techniques that are applied to pseudo-NMOS. Section IV presents the simulation results of the logic circuits with and without the power reduction techniques and section V gives the conclusion.

II. Pseudo-NMOS Logic

Pseudo-NMOS logic is an example of ratio-ed logic which uses a grounded PMOS load and an NMOS pull-down network that realizes the logic function [5]. The main advantage of this logic is it uses only N+1 transistors verses 2N transistors for static CMOS. In this logic the high output voltage for any gate is Vdd and the low output voltage is not 0volt. This results in decreased noise margin. The main drawback of this logic is very high static power consumption as there exists a direct path between Vdd and ground through the PMOS transistor. In order to make low output voltage as small as possible, the PMOS device should be sized much smaller than the NMOS pull-down

devices. But to increase the speed particularly when driving many other gates the PMOS transistor size has to be made larger. Therefore there is always a trade-off between the parameters noise margin, static power dissipation and propagation delay. In the implementation of NAND and NOR gates in Pseudo-NMOS logic, the PMOS transistors are of equal size and the size of NMOS transistors in NAND logic is larger than the NMOS transistors in NOR gates for the same performance. Because of high static power dissipation this logic is used to build fast wide NOR gates. Fig. 1, 2 and 3 show the circuit of ratio-ed Pseudo-NMOS NAND gate, NOR gate and inverter for a 4:1 current ratio.

Figure 1. Pseudo-NMOS NAND gate

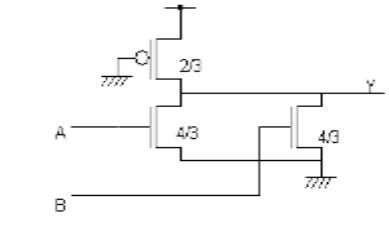

Figure 2. Pseudo-NMOS NOR gate

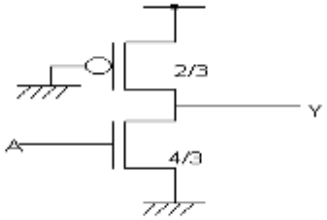

Figure 3. Pseudo-NMOS inverter

III. Proposed static power reduction techniques

In this section the methods used for decreasing static power in Pseudo-NMOS logic such as reverse body bias (RBB) and transistor stacking are described.

A. *Reverse body bias*

This is an effective approach to reduce leakage power. In this method, when the circuit enters the standby mode, reverse body bias is applied to increase the threshold voltage Vt of the transistors and this decreases the sub-threshold leakage current. Vt is related to the reverse bias voltage between the source and body Vsb by the following Eq. (4) .

$$Vt = Vto + \gamma \{(\sqrt{2\phi_f + |Vsb|}) - (\sqrt{2\phi_f})\} \qquad (4)$$

Where Vto is the zero bias Vt for Vsb = 0volt, ϕ_f is a physical parameter and γ is a fabrication-process parameter [6]. Modification of Vt can be achieved by changing |Vsb|. This method can be either applied at the full chip level or at a finer granularity. The advantage of this method is that it can be implemented without incurring any delay penalty [7]. The key issue is that the range of threshold adjustment is limited, which in turn limits the amount of leakage reduction.

B. *Transistor stacking method*

Transistor stack is a leakage reduction technique that works both in active and stand-by mode. It is based on the observation that two off-state transistors connected in series cause significantly less leakage than a single device. This effect is known as the "Stacking Effect". When two or more transistors that are switched OFF are stacked on top of each other [Refer Fig. 4], then they dissipate less leakage power than a single transistor that is turned off. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage. Hence Therefore in Fig. 4 transistor T2 leaks less current than transistor T1 and T3 leaks less than T2. Hence the total leakage current through the transistors T1, T2 and T3 is decreased as it flows from Vdd to ground. So Ileak1 is less than Ileak2 [8]. If natural stacking of transistors do not exist in a circuit, then to utilize the stack effect a single transistor of width W is replaced by two transistors each of width W/2 [9]. The leakage reduction achievable in a two-stack comprising of devices with widths w_u and w_l compared to a single device of width w is given by Eq. 5 & Eq. 6.

$$X = \frac{I_{device}}{I_{stack}} = \frac{w}{w_u^{\alpha} w_l^{1-\alpha}} 10^{\frac{\lambda_d V_{dd}}{s}(1-\alpha)} \qquad (5)$$

$$\text{Where } \alpha = \frac{\lambda d}{1+2\lambda d} \qquad (6)$$

λ_d is the drain-induced barrier lowering (DIBL) factor and s is the sub-threshold swing co-efficient [10].
When $w_u = w_l = w/2$ then the leakage reduction factor or stack effect factor *X* is rewritten as

$$X = \frac{w}{\frac{w}{2}^{\alpha}\frac{w}{2}^{(1-\alpha)}} 10^{\frac{\lambda_d V_{dd}}{s}(1-\alpha)} \qquad (7)$$

$$X = 2 \times 10^{\frac{\lambda_d V_{dd}}{s}\left(\frac{1+\lambda_d}{1+2\lambda_d}\right)} \quad (8)$$

$$X = 2 \times 10^{u} \quad (9)$$

Where u is the universal two-stack exponent that depends only on the process parameter, λ_d and s, and the design parameter V_{dd}. Thus the leakage current through a single OFF device is greater than leakage through a stack of two OFF devices.

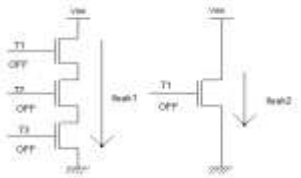

Figure 4. Transistor stack effect

IV. Simulation results

In this work, the static power analyses of Pseudo-NMOS logic gates are carried out in 65nm and 45nm process technology. Initially the static current of the gates is computed without any reduction technique (Base case). Then the proposed methods reverse body bias and transistors stacking are applied to the gates separately and then a combination of the two techniques is applied to the gates. The net lists of the circuits are extracted and simulated with BSIM4 models of MOSFET [11]. The simulations are done in HSPICE with two different supply voltages of 1.0v (strong inversion) and 0.3v (sub-threshold region) at a temperature of 27º C. The simulation results are shown in Table I , Table II for NAND gates and Table III & Table IV for NOR gates. In 65nm and 45nm technologies, static power of NOR gates is higher than NAND gates. The reduction in static power is more in the sub-threshold region. In all the gates the static power reduction is more for the combined effect of stack and RBB techniques in both the strong inversion and sub-threshold region. Fig 5 and Fig 6 shows the % reduction in static power in 65nm and 45nm respectively.

TABLE I. STATIC CURRENT IN PSEUDO-NAND GATE AT 65NM

S.No	Reduction technique used	Static current (A)	
		Vdd = 1.0v	Vdd = 0.3v
1	Base case	47.28E-06	159.3E-09
2	Stack	10.94E-06	32.86 E-09
3	RBB	42.95E-06	66.49 E-09
4	Stack+RBB	9.790E-06	13.69E-09

TABLE II. STATIC CURRENT IN PSEUDO-NAND GATE AT 45NM

S.No	Reduction technique used	Static current (A)	
		Vdd = 1.0v	Vdd = 0.3v
1	Base case	40.53E-06	84.45E-09
2	Stack	18.18E-06	29.49E-09
3	RBB	37.10E-06	36.78E-09
4	Stack+RBB	16.35E-06	12.35E-09

TABLE III. STATIC CURRENT IN PSEUDO-NOR GATE AT 65NM

S.No	Reduction technique used	Static current (A)	
		Vdd = 1.0v	Vdd = 0.3v
1	Base case	97.34E-06	327.04E-09
2	Stack	23.06E-06	69.37E-09
3	RBB	88.39E-06	136.75E-09
4	Stack+RBB	20.65E-06	28.92E-09

TABLE IV. STATIC POWER IN PSEUDO-NOR GATE AT 45M

S.No	Reduction technique used	Static current (A)	
		Vdd = 1.0v	Vdd = 0.3v
1	Base case	84.23E-06	178.28E-09
2	Stack	18.47E-06	29.75E-09
3	RBB	77.14E-06	76.78E-06
4	Stack+RBB	16.59E-06	12.39E-09

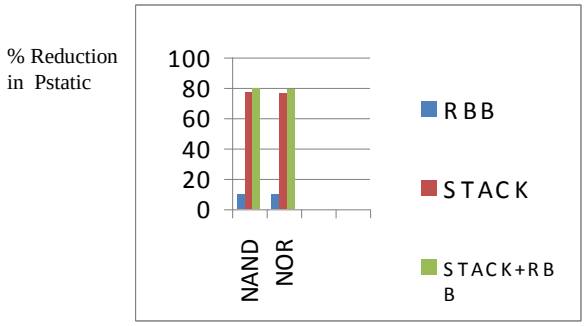

Figure 5(a). % Pstatic reduction at 65nm, 1V

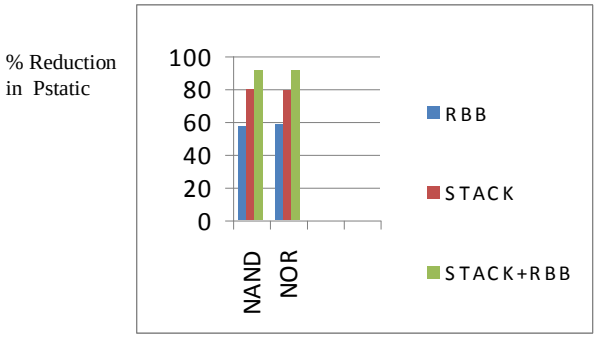

Figure 5(b). % Pstatic reduction at 65nm, 0.3V

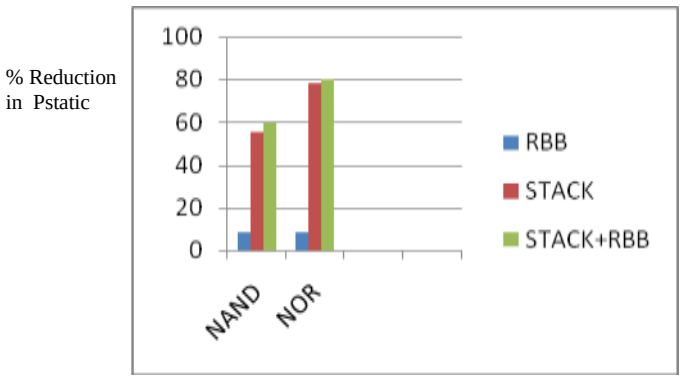

Figure 6(a). % Pstatic reduction at 45nm, 1V

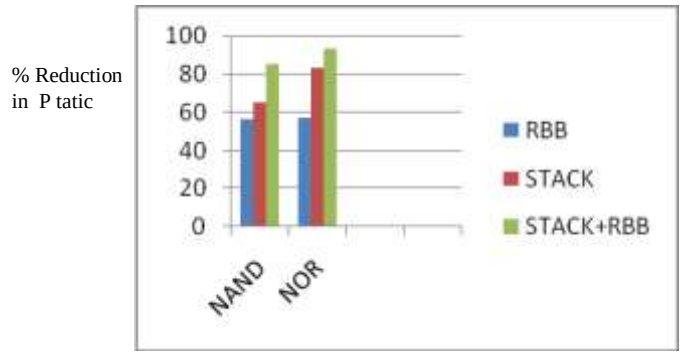

Figure 6(b). % Pstatic reduction at 45nm, 0.3V

v. Conclusion

Static power reduced pseudo-NMOS logic gates are proposed in this work. The circuits are analyzed in 65nm and 45nm process technology with BSIM4 models of MOSFET. The simulations are done with two different supply voltages of 1volt and 0.3volt. In all the gates the static power is decreased with both the reduction methods. In both the technologies, the combined effect of reverse body bias and stacking results in least static power consumption. In 65 nm process technology maximum static power reduction of 91.39 % is observed in NAND gates and in 45 nm technology NOR gates have the highest reduction o 93.04% at sub-threshold operation.

References

[1] L. Junming, S. Yan, L. Zhenghui and W. Linging , "A Novel 10-Transistor Low-Power High-speed Full Adder cell", Proc. of IEEE 6th International Conference Solid State and Integrated Circuit Technology, pp. 1155-1158, 2001.

[2] A.M. Shams and Gu. M. Zhang, "A Review of 0.18µm Full Adder Performances for Tree Structure Arithmetic Circuits", IEEE Trans. Very Large Scale Integrating (VLSI) systems, Vol. 13 , No. 6, pp. 686-695, 2005.

[3] Yang Pan Liu, Robert P. Dick, Li Shang and Huazhang, "Accurate Temperature Dependent Integrated Circuit Leakage Power Estimation is Easy", EDAA 2007.

[4] International Technology Roadmap for Semiconductors: www.itrs.net/Links/2005ITRS/Design 2005.pdf.

[5] Rabaey J. ,"Digital Integrated Circuits-A Design Perspective", Prentice Hall, 1996.

[6] Liang yu Loy, Weijia Zhang, Zhi-Hui Kong, Wang-Ling Goh and Kiat-seg-Yeo, "Body-Boootstrapped Buffer Circuit for CMOS Static Power Reduction", IEEE 2008.

[7] J. Tschanz, S. Narendra, Y. Ye, B. Bloechel, S. Borkar, V.De, "Dynamic Sleep Transistor and Bodybias for Active Leakage Power Control of Microprocessors", IEEE Journal of Solid State Circuits, Vol.38, No.2, pp.1838-1845 , November 2003.

[8] Vasanth Venkatachalam and Michael Franz, "Power Reduction Techniques for Microprocessor Systems", ACM Computing Surveys, Vol .37, No. 3, pp.195-237 , September 2005.

[6] [9] M.C. Johnson, D.Somasekhar, L.Y. Chiou, and K.Roy ," Leakage Control with Efficient Use of transistor Stacks in Single threshold CMOS," IEEE Trans. Very Large Scale Integrating (VLSI) systems, Vol. 10 , No. 1, pp. 1-5, 2002.

[10] Siva Narendra, ShekharBorkar,Vivek De, Dimitri Antoniadis, and AnanthaChandrakasan , " Scaling of Stack Effect and its Application for Leakage Reduction", pp. 195-200, ISLPED 2001.

[11] http://www- device.eecs.Berkeley.edu/~ptm/mosfet.

Biographies

Ms. M. Janaki Rani received her B.E. degree from Annamalai University, Tamil Nadu, India and M.E. degree in Electronics from MIT, Anna University, Chennai, India. She has around 18 years of teaching experience. Currently she is doing her research in the area of low power VLSI Design in Sathyabama University, Chennai. Her research interests include Low power VLSI design, VLSI signal processing, advanced digital system design and embedded system design. She has published many papers in national and international conferences & journals.

Dr.S.Malarkkan, Principal in Manakula Vinayagar Institute of technology, Puducherry obtained his B.E. Degree from Thiagarajar College of Engineering, Madurai in the year 1988 and M.E. Degree in Optical Communication and Ph.D in Wireless & Mobile Communication from College of Engineering, Anna University, Chennai. He has over 22 years of experience in teaching and his area of interest includes analog and digital communication, mobile communication and wireless networks. He is a life member of ISTE, CSI and a fellow of IETE. He was serving as a member in IETE Executive Committee, Chennai zone from 2006 to 2008.