Design of a High Slew Rate Moderate Speed CMOS Opamp

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***Abstract*— In this work, a high slew rate CMOS operational amplifier (op-amp) having moderate speed is presented which operates at supply voltage of 1.8 V (rail to rail) using TSMC 0.18 µm CMOS technology. Current buffer compensation strategy in conjunction with Miller compensation is used to achieve high speed and high slew rate. In this design, a tradeoff between speed and power dissipation is maintained. The op-amp is designed to exhibit a unity gain frequency of 1.1 GHz and gives a gain of 60 dB with a 57.50º phase margin. The proposed design exhibits a higher unity gain bandwidth and slew rate as compared to other conventional methods at the same load [1], [2]. This opamp is designed for high speed applications where a higher slew rate is required.**

Keywords- Current Buffer, High Frequency, Low Voltage, Operational amplifier, slew rate

I. INTRODUCTION

VLSI technology continues to scale to ever smaller transistor sizes to include more transistors in DRAM and increase microprocessor speed. This scaling puts many limitations to analog device design due to smaller sizes and lowered supply voltage. As the transistor lengths decrease in size, the channel length modulation increases drastically and drain current increases much more with a larger V_{DS}. To develop efficient and high speed devices, the circuit designers are forced to work in the low voltage and low power regime. There is a tradeoff between speed and power. Also, if the speed of a circuit is increased to a large extent, the overall gain of the design is severely degraded. Moreover, as the supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the voltage headroom available.

The reported high frequency and low power voltage amplifiers using classical schemes have good small signal characteristics, but their bandwidth and slew rate is relatively low. A two stage CMOS op-amp design procedure suitable for hand calculation and analysis is given by Allen and Holberg [13]. Ahuja [9] devised an improved compensation technique having large advantages over the conventional RC compensation network which can drive large capacitive loads up to 100 pF. However, it requires a larger power supply and the op-amp operation is somewhat slow. Palmisano and Palumbo [7] devised a current buffer compensation scheme which results in a noticeably large improvement in bandwidth as compared to nulling resistor or voltage buffer compensation techniques. Also, it improves the PSRR and does not degrade the amplifier output swing and results in an efficient compensation with lower values of compensation capacitance. In the approach by Gangopadhyay and Bhattacharyya [4] a high bandwidth of 2.3 GHz has been obtained, but the power consumed by the opamp is somewhat higher at 25 mW. Ahmed Younis and Marwan Hassoun [5] designed a fully differential opamp having a large gain as well as a high bandwidth but power consumption was larger. Boaz Shem-Tov et.al. [3] used negative miller capacitance compensation technique and obtained a respectable gain and used a large load capacitance, but the unity gain bandwidth was not quite high. This work is mainly motivated from the fact that high frequency op-amp designs in the gigahertz range are often reported with adequate dc gain, but slew rate is never reported to be higher than 400-500 V/µs. The idea is to increase the output stage transconductance to such a value that the circuit can drive a load capacitance at a much faster rate to its final voltage level and also bring about its discharge at a faster rate. Moreover, it is also aimed to achieve a higher bandwidth with a respectable gain and power dissipation.

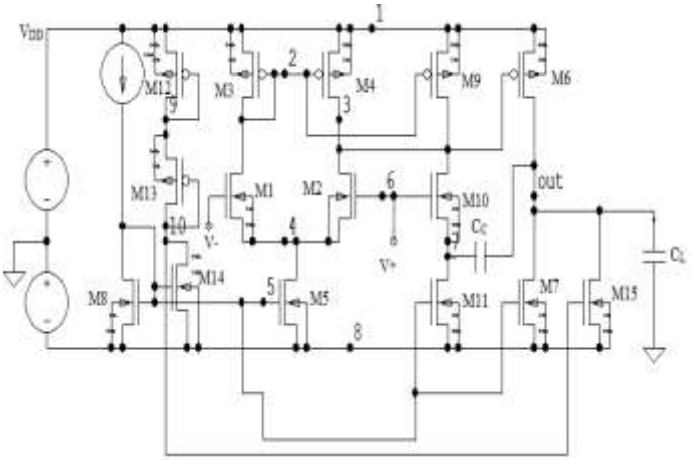

Figure 1. Circuit diagram of the proposed op-amp

II. DESIGN PRINCIPLE

MOS devices when operated in saturation region, their current is almost constant (neglecting lambda effect). The bias circuit is in general a current mirror with a reference current I_{ref} considered to be an ideal current source. This paper employs an indirect compensation technique using a common gate stage. The design is a two-stage op-amp with current buffer compensation. The circuit diagram is as shown in fig.1.

The circuit comprises of the following stages:

A. Differential gain stage

It comprises of transistors M1 to M4. The gate of M1 is the inverting input and that of M2 is the non-inverting input. The transconductance of this stage is simply the transconductance of M1 or M2. M3 and M4 are the active current mirror load transistors of the differential amplifier. The current mirror topology performs the differential to single-ended conversion of the input signal and it also improves common mode rejection ratio.

B. Second gain stage

Consisting of transistors M6, M7 and M15 this stage takes the output from the drain of M2 and amplifies it through M6 which is in the standard common source configuration. Again, similar to the differential gain stage, this stage employs a parallel combination of active device M7 and M15 (in order to increase output transconductance) to serve as the load resistance for M6. This transconductance improves the load driving capability of the circuit to a large extent.

C. Current buffer stage

It consists of transistor M_{10} with transistors M_9 and M_{11} operating in saturation acting as ideal current source and sink, respectively. The output is fed back to the input of second stage i.e. to gate of M_6 via C_C and M_{10}.

D. Bias string

It consists of an ideal current source together with transistors M_8, M_5, M_{12}, M_{13}, M_{14}, M_7 and M_{15}. M_8 is diode connected to ensure that it operates in saturation. The aspect ratios of M_{12} and M_{13} are selected in such a way that M_{15} always remains in saturation.

Two stage CMOS op-amps adopt Miller compensation to achieve stability in closed loop conditions to cancel a non-dominant left half plane pole with the right half plane zero. But the design is not always reliable as the pole-zero cancellation may not be accurate and a pole-zero doublets may result. The uncompensated right half plane zero arises due to the forward path through the compensating capacitor (Cc) to the output. It makes a negative phase contribution to the open-loop gain at a relatively high frequency and drastically reduces the maximum achievable gain bandwidth. We have used a nulling resistor compensation in which the output is fed back through nulling resistor R_C and coupling capacitor C_C to input of second stage and a current buffer compensation in which the output is fed back to input of second stage through coupling capacitor C_C and transistor M_2, which acts as a current buffer.

III. SIMULATION RESULTS

In order to examine the proposed compensation strategy, the two-stage op-amp was designed using the model parameter of TSMC 0.18µm CMOS process. This circuit operates efficiently in a closed loop feedback system, while high bandwidth makes it suitable for high speed applications. The simulations were carried out using Tanner spice simulator. The simulated results are tabulated and a comparison is made as shown below:

Circuit operating conditions:

Operating Temperature = room temperature; Power supply= 1.8 V, Input bias current = 45 µA, C_L= 1 pf.

TABLE I. RESULTS AND COMPARISON

Sl.no.	Specifications	Our design	[1]	[2]	[3]
1	Technology	0.18µm CMOS process	0.18µm	0.18µm	0.18µm
2	Supply voltage	1.8v rail-to-rail (±0.9v)	1.8 V	1.5V	1.8V
3	Load capacitance (C_L)	1pF	1pF	1pF	2pF|| 1KΩ
4	UGB	1.1GHz	312Mhz	236Mhz	392Mhz
5	Phase Margin	57.5 degrees	56 degrees	81.3 degrees	73 degrees
6	Output swing	1.68v (-0.9 to 0.78v)	1.65v diff swing	1.26v	
7	DC gain	60dB	95dB	92.5dB	86dB
8	ICMR	-0.752 to 0.726 v			
9	|PSRR+|,|PSRR-|	60dB, 64dB	70dB		
10	|CMRR|	52dB	70dB		
11	Power consumption	686.46µW	500µW	50µW	12mW
12	Slew rate +, Slew rate -	1210 v/µs, -385.9 v/µs		16.75 v/µs	

IV. SIMULATED CURVES

Fig. 2 shows the DC transfer curve. The offset voltage is very small, 0.009 mV. For the frequency response plot, an ac signal of 1V is swept with 10 points per decade from a frequency of 1 Hz to 4 GHz. Fig. 3 shows the DC gain (in dB) versus frequency in Hz (in log scale) and fig. 4 shows the Phase curve of opamp in open loop configuration. The DC gain of the opamp is 60 dB; unity gain bandwidth is 1.1 GHz with a

phase margin of 57.5º which is good enough for an op-amp operating at a high frequency as compared to some conventional designs [1], [2], [3].

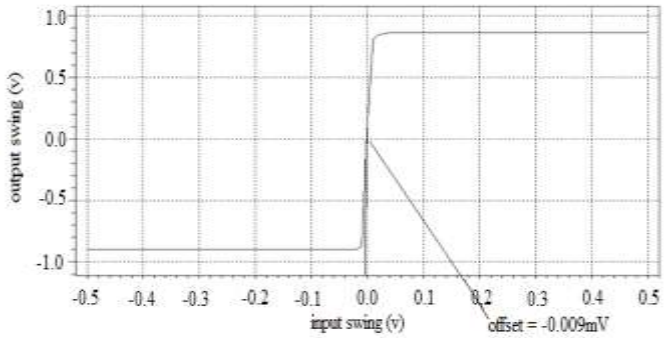

Figure 2. DC transfer curve

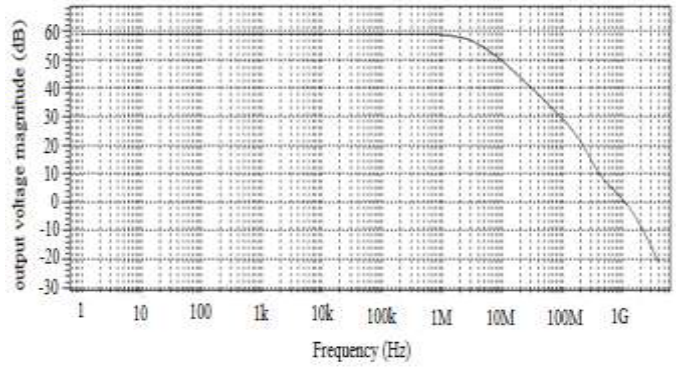

Figure 3. Gain vs frequency curve

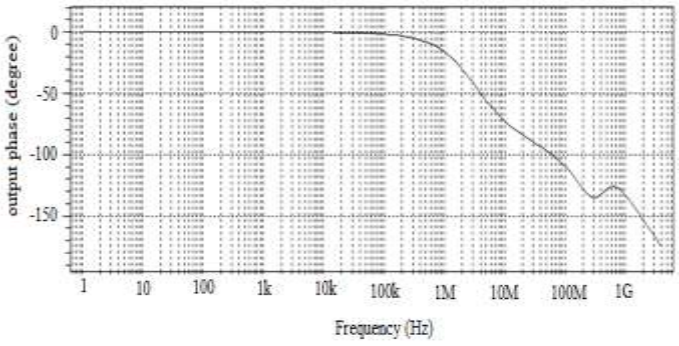

Figure 4. Phase vs frequency curve

Fig.5 shows the output noise spectral density of the opamp. It has a value of 2 µv/sqrt (Hz) at dc and 1.25 µv/sqrt (Hz) at a frequency of 10 Mhz.

The circuit has an input common mode range (ICMR) from -0.752 V to 0.726 V which is shown in fig. 6. The ICMR nearly covers the whole rail to rail voltage range. Fig. 7 shows the common mode rejection ratio (CMRR) response of the op-amp.

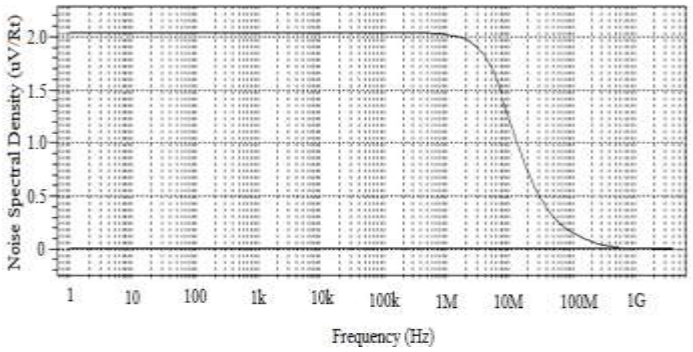

Figure 5. Output noise characteristics

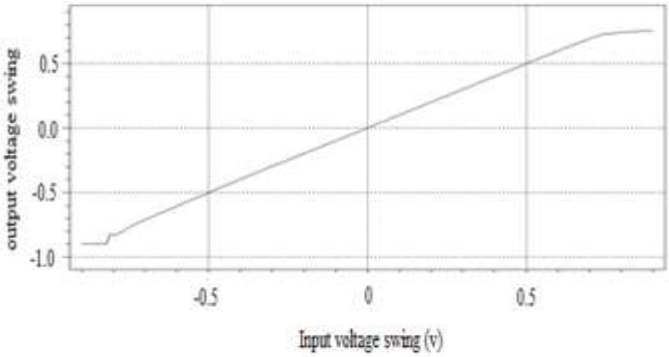

Figure 6. ICMR

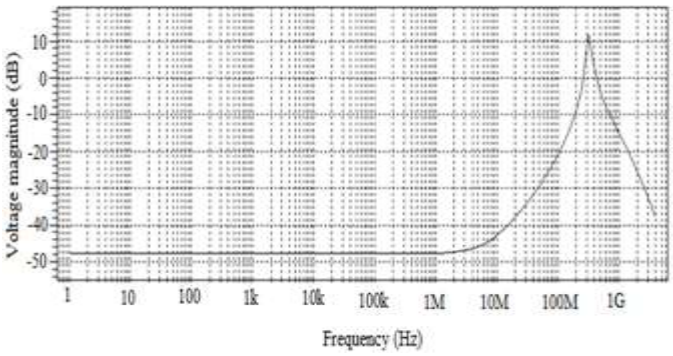

Figure 7. CMRR

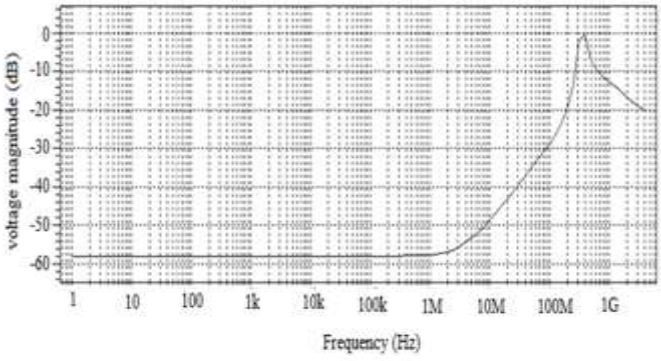

Figure 8. PSRR+

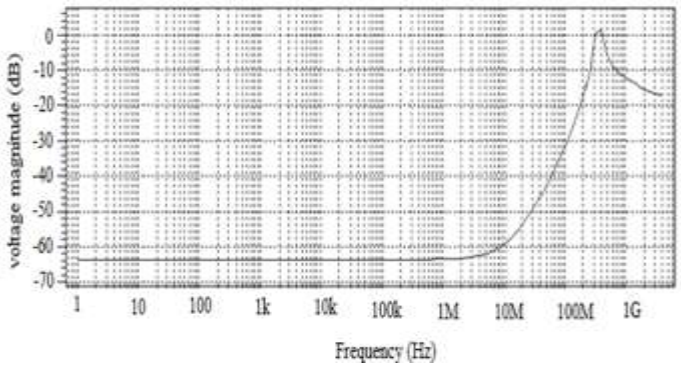

Figure 9. PSRR-

The graph evaluating the positive power supply rejection ratio (PSRR+) of the op-amp in dB is shown in fig. 8. It shows the influence of the positive power supply ripple on the op-amp's output. Similarly, the negative power supply rejection ratio (PSRR-) curve is also shown in fig. 9.

Fig.10 shows the slew rate performance of the opamp. The slew rate (+ve and –ve) are found to be 1210 V/µs and -385.9 V/µs respectively, which is quite good as compared to other designs that drive a capacitive load of 1 pF or higher. The positive slew rate is large because the output stage Transconductance is large enough and M_6 can provide adequate current required for building up the output voltage. The negative slew rate is smaller due to the limited current discharge rate through the load capacitor C_L.

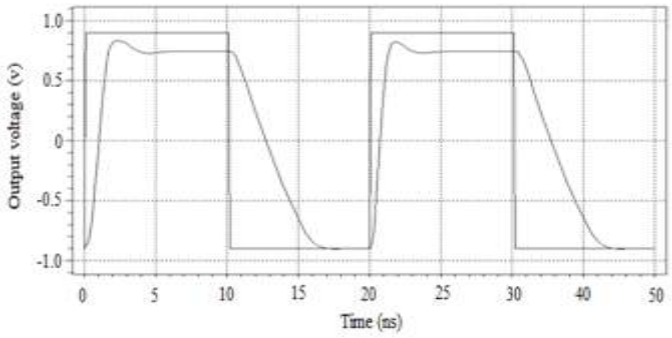

Figure 10. Slew rate of the op-amp

V. CONCLUSION

This work uses a current buffer compensation strategy in conjunction with Miller compensation for a two stage CMOS op-amp with an aim to achieve high speed and high slew rate. The increase in unity gain bandwidth has been achieved by increasing the output transconductance and lowering the compensation capacitor value and by increasing the bias current to some extent. As a tradeoff, the DC gain has decreased to some extent and the power consumption has slightly increased. Further, the circuit is designed in such a way so that the output stage transconductance is increased so that the gain maintains a respectable value even at higher frequencies. The slew rate is found to be higher than reported high frequency designs at 0.18 µm CMOS technology. Therefore, this opamp can be used in high frequency applications and for driving capacitive loads at a faster rate.

REFERENCES

[1] P.E. Allen and D.R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.

[2] Ehsan Kargaran, Hojat Khosrowjerdi, Karim Ghaffarzadegan, "A 1.5 V High Swing Ultra-Low-Power Two Stage CMOS OP-AMP in 0.18um technology", 2010 2nd International Conference on Mechanical and Electronics Engineering (ICMEE 2010).

[3] Boaz Shem-Tov, Mücahit Kozak, and Eby G. Friedman, "A High-Speed Cmos Op-Amp Design Technique Using Negative Miller Capacitance."

[4] Daibashish Gangopadhyay, T.K. Bhattacharyya,"A 2.3 GHz gm-boosted High Swing Class-AB Ultra-Wide Bandwidth Operational Amplifier in 0.18µm CMOS."

[5] Ahmed Younis' and Marwan Hassoun,"A High Speed Fully Differential CMOS Opamp."

[6] Ratul Kr. Baruah, "Design of a Low Power Low Voltage CMOS Opamp", International Journal of VLSI design & Communication Systems (VLSICS) Vol.1, No.1, March 2010.

[7] G. Palmisano and G. Palumbo "A Compensation Strategy for Two-Stage CMOS opamps Based on Current Buffer"; IEEE Transactions on circuits and systems—I: Fundamental theory and applications, Vol. 44, No. 3, March. 1997.

[8] J. Mahattanakul, *Member, IEEE*, "Design Procedure for Two-Stage CMOS Operational Amplifiers Employing Current Buffer", IEEE Transactions on circuits and systems—II: Express Briefs, vol. 52, no. 11, November 2005.

[9] Bhupendra K. Ahuja,"An Improved Frequency Technique for CMOS Operational Amplifiers", IEEE Journal of solid-state circuits, VOL. SC-18, *no.* 6, December 1983.

[10] Yavari, M., Maghari, N. and Shoaei, O. (2005) "An Accurate Analysis of Slew Rate for Two stage CMOS Opamps". IEEE Transactions on Circuits and Systems - II: Express Briefs 52, pp. 164-167.

[11] R. Jacob Baker and Vishal Saxena, Department of Electrical and Computer Engineering, Boise State University, "High Speed Op-amp Design: Compensation and Topologies for Two and Three Stage Designs."

[12] Mohammad Yavari, *Student Member, IEEE*, Nima Maghari, and Omid Shoaei, "An Accurate Analysis of Slew Rate for Two-Stage CMOS Opamps", IEEE Transactions on circuits and systems—II: Express Briefs, VOL. 52, no. 3, March 2005.

[13] B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2002.

[14] P.E. Allen and D.R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.