Efficient transporting Ethernet traffic through SONET/SDH networks

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Abstract: **The communication landscape is denoted by two differing technologies: Ethernet in LAN and SONET/SDH in WAN. To interface the LAN to WAN, as Ethernet is not directly supported over the SONET/SDH network. And also due to transporting rate mismatch make carrying Ethernet connection over a SONET pipe bandwidth inefficient. For Efficient transporting Ethernet traffic through SONET/SDH networks new technologies have been standardized, VC and GPF, which are features of next generation SONET/SDH.**

This paper presents the study of virtual concatenations, Generic Framing Procedure and implementation of SONET/SDH line card. A key attribute of these designs is the support for the VC and LCAS standards.
Keyword - SONET, SDH, ROI, VC, GPF, LCAS

INTRODUCTION

In year 2000, Telecommunication has shifted from the traditional voice transport to data transport. Instead of an evolution of the existing transport standards, an evolution was necessary to enable the additional data related transport and its need to share the concept on the new SDH/SONET concepts. Today SDH/SONET is the deployed technology in the core network with huge Investment in capacity. Ethernet is the dominant technology of choice at LANs and WAN. Data traffic is still growing, but only at slower speed than expected. For long term all the network topologies focusing on an IP/Ethernet only approach are shifting. So the today's future is bringing SDH/SONET and ETHERNET together.

The customer expects from the operator: Quality of service & bandwidth at lower costs, native data interfaces and use & improve what he knows. On the other hand operator wants: reduce operational costs, realize revenue-earning service, use bandwidth of core network, low investment, immediate ROI and close the edge bottleneck. So, to solve all these problem of customers and operator is to make SDH/SONET flexible and data aware at the edge and still use the existing core.

All global carriers count on SONET/SDH as their transport infrastructure [4], and have gained tremendous experience operating, maintaining, and deriving revenue from this network. Until recently, SONET/SDH systems were optimized for TDM traffic that fits into strict well-defined bit rates. In order to transport data in an efficient manner over the existing infrastructure more flexibility is needed. This led to the development by ANSI/ITU of Virtual Concatenation (VC) and Link Capacity Adjustment Scheme (LCAS) standards [1]. Deployment of equipment that implements these standards will further extend the adoption of SONET/SDH networks

Virtual concatenation

Virtual concatenation is a mechanism that provides flexible and effective use of SONET/SDH payload. Historically, SONET/SDH was first defined as a (worldwide) unified digital hierarchy for the transport of 64-kb/s-based TDM service. The capacity of payload was rigidly defined for plesynchronous digital hierarchy (PDH) service accommodation. However, the disadvantages of such a rigid SONET/SDH rate hierarchy, especially when data applications such as Ethernet are considered, were soon realized. Virtual concatenation breaks the limitation incurred by this rigidity via the definition of payloads with flexible bandwidth. It "virtually" concatenates several payloads to provide a payload with flexible bandwidth, appropriate for data service accommodation

The Virtual Concatenation is specified in ITU-T Recommendations G.707[2]. Virtual concatenation (VCAT) is an inverse multiplexing technique used to split SONET/SDH bandwidth into logical groups, which may be transported or routed independently. Virtual Concatenation is used to split SONET/SDH bandwidth up into right-sized groups. These Virtual concatenation is considered the primary enhancement to voice optimized SONET/SDH, in order to support the transport of variable bit data streams. Other recent SONET/SDH enhancements include Link Capacity Adjustment Scheme (LCAS), and the Generic Framing Procedure (GFP)[3]. In conjunction with LCAS and GFP, Virtual Concatenation gives the advantage of splitting the required bandwidth equally among a set number of sub paths called Virtual Tributaries (VT).Several Virtual Tributaries, form part of a Virtual Concatenation Group (VCG). VCAT works across the existing infrastructure and can significantly increase network utilization by effectively spreading the load across the whole network.

LINK CAPACITY ADJUSTMENT SCHEME

As described in the last section, virtual concatenation can be applied to construct payloads with various capacities. Although the number of concatenated payloads can be determined in advance for most applications, it may be useful to allow the number of concatenated payloads to be changed dynamically. LCAS is defined for this purpose. In LCAS, signaling messages are

Exchanged between the two VC endpoints to determine the number of concatenated payloads. For instance, assume STS-5v SPE/VC-3-5v (250 Mb/s payload capacity) is currently used. According to user requirements, the number of concatenated payloads, currently five, could be
increased to obtain STS-6v SPE/VC-3-6v, or reduced to obtain STS-4v SPE/VC-3-4v. Furthermore, LCAS makes sure that this process is done in a hitless manner (i.e., without any bit errors during the process). Therefore, LCAS allows carriers to assign and utilize bandwidth more efficiently and flexibly. This feature is very useful, for instance in adjusting bandwidth requirements on a time-of-day basis, across certain routes for which traffic variability is predictable and seasonal. Another application is the rerouting of traffic due to current network conditions, such as failures or maintenance procedures.

Link Capacity Adjustment Scheme (LCAS), specified by the G.7042 specification[1], can be viewed as a further enhancement of VC, and is defined as an adjustment scheme that hit lessly increases or decreases the capacity of a container that is transported in a SONET/SDH/OTN network using VC.
Therefore LCAS offers network designers the ability to automatically fine tune the bandwidth .
*Why VC and LCAS :*There is no growth in Ethernet over SDH because of low investment by the user. For users, the added value is high: a reliable, high performance WAN connection that is as simple to manage as any other port on their LAN and whose bandwidth can be matched to their needs.

SONET FRAMES TO ETHERNET FRAMES

A translation engine is provided for efficiently translating SDH/SONET frames[5] (101) to Ethernet frames (105) and vice versa. In accordance with one embodiment, a translation system includes a buffer (103) for holding SDH/SONET (101) and Ethernet frames (105). An Ethernet Media Access Control (MAC) address for a corresponding SDH/SONET TDM slot (103 E-103 F) further provided. A translation engine for translating SDH/SONET frames (101) into Ethernet frames (105) is in communication with an output interface. The SDH/SONET payload (101 A) is sent through a translation engine to translate the SDH / SONET payload (101 A) into an Ethernet payload (105 A). For translating from Ethernet to SDH / SONET, a reverse process occurs

ETHERNET OVER SONET/SDH LINE CARDS

The VC and LCAS standards allow the service provider to provide many price points for transmission of this data because the data can be sent over a multiple number of STS-1 or STS-3c. Today data is usually only offered at the contiguous concatenation bandwidths of STS-3C, STS-12C, etc.

A next generation Ethernet over SONET/SDH line cards would integrate all the functions needed to interface to both SONET/SDH and Ethernet networks. The SONET/SDH interface could be a backplane interface to an STS-1 switch fabric or it could be a line interface to a SONET/SDH ring, while the client side of the card would interface to multiple 10/100/1000 Ethernet ports.

The hardware and software implementation of a typical Ethernet over SONET/SDH line card will be described by the following blocks:

a) Ethernet Gigabit MACs and PHYs

b) VC/LCAS/GFP Mapper

c) SONET/SDH Framer

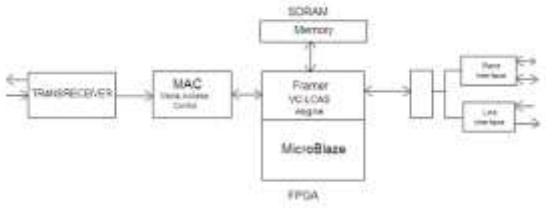

Fig. : Next Generation Line Card

Incoming Ethernet traffic would first be processed by the Ethernet MAC and then encapsulated by mapper into GFP (Generic Framing Procedure)[7] packets mapper. GFP offers an alternative to byte level HDLC which contains a header that can detect double bit errors and correct single bit errors and can be provides for variable length packets. GFP also defines a transparent mapping for any 8B/10B block coded protocol and this allows storage protocols to pass through the network. The GFP frame mapper can support fractional bandwidth rates because it strips out idles between packets but the transparent mapper needs to reserve full bandwidth end to end. The GFP mapper would forward the data to a logic block for inverse muxing.

1.) VC/LCAS/GFP Mapper:

Mapping is the process of insertion of overhead and pointer information in payload for the generation of

STM frame. A mapper perform following functions- Insertion of AU pointers. Insertion of path overhead in payload. Insertion of Regenerator section Overhead bytes and Multiplexer Section Overhead for formation of STM Frame.

2.)MICROBLAZE:

Micro Blaze[11] embedded soft core is a 32 bit Reduced Instruction Set Computer (RISC) optimized for implementation in Xilinx FPGA devices. Both instruction and data interface of Micro blaze are 32 bit wide and use big endian bit reversed for format. There are 32 general purpose registers, 32-bit instructions with three operands and two addressing modes. This soft core, by virtue of massively parallel General Purpose Input and Output (GPIO) configurability and access to various embedded cores, provide new alternatives for creating high performance applications.

3.) SONET/SDH Framer :

The circuitry for a word aligner[9] is very simple, an example for a 16-bit data path is shown in

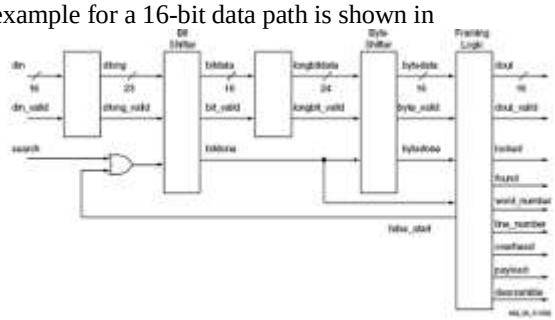

Figure : 16 bit data path Block Diagram

Assuming the incoming data is initially unaligned, operation is initiated by the search input being asserted for one or more cycles. Once the search input transitions Low, searching for the frame header data can start. The incoming 16-bit data word is combined with the lower seven bits of the data word from the previous cycle, and then fed into a bit-shifter module .The bit shifter contains 16-bit comparison logic to test for the presence of the A1A1 bit pattern (0XF6F6h) in any of the eight possible positions of the 23-bit input word. If the A1A1 is found in the same position on two consecutive cycles, assumes the first part of the frame header period of the frame is found. There are 48 consecutive A1 bytes in an OC48 frame header. The encoder generates a 3-bit signal to shift the incoming data word from 0 to 7 bit positions. The incoming data is now assumed to be bit aligned, and the bit-valid flag is raised.

The byte shifter contains 8-bit comparison logic that searches for both the A1 octet (0XF6h) and the A2 octet (0X28h once the bit-done input has gone high and the input data can be assumed to be bit-aligned. If the search logic finds the pattern A1A2 in either of the two possible positions (bits [23:8] or [15:0]), it is assumed that this is the A1A2 transition in the frame header, and the byte_done flag is asserted. The encoder will generate a one-bit signal that shifts the incoming data either 0 or 8-bit positions, so that the output data is precisely aligned on the A1A2 boundary. The output will therefore be A1A1 followed by A2A2.

The byte-aligned data is now fed to the framing logic. This again performs a comparison looking for the A1A2 transition. If this transition is found in the correct place, three times running, then the signal "locked" will be asserted. In addition, each time the A1A2 transition is found, the found signal will be asserted for one clock cycle. If the transition is not found in the correct place, then the false-start signal is used to reset all the logic, and the search begins

again. The value n is determined by a constant in the code, and default value of "3". Found implies that the circuit finds an A1A1 word immediately followed by an A2A2 word. The "correct place" is determined by the type of data that is being received, and the basic 8 KHz rate of telecom systems. In the case of OC48, the A1A2 transition should occur every38,880 octets (19,440 clocks assuming 16-bit wide data.) Once alignment is achieved the output signals available are:

word-number: This is the word number of the current data (0 to 2159 for OC48) line-number: This is the line the word is in (0 to 8).

overhead: This indicates the receipt of the overhead portion of the frame.

payload: This indicates that the word is part of the payload.

descramble: This is used to enable and disable the scrambling logic. Once locked, the circuit continues in operation until either a search command is issued to it, or an A1A2 is not found in the correct place for m consecutive cycles.

The members of a VC group map directly to SONET/SDH tributaries. Additional Path Overhead bytes (C2, J1, G1, B3) would be added to the SONET/SDH tributaries and then they are either sent out onto an internal SONET/SDH backplane or further processed for the line and section overhead bytes. Equipment that provides SONET/SDH switching, connect the line cards to the working and protection switch fabrics using high-speed serial lines. These serial lines run at 622 Mbps or at 2.488 Gbps. The Egress data path follows the reverse process.

In this data path SONET/SDH frames would be stored externally to the device in SDRAM. The SDRAM buffers the fastest arriving paths. The VC standard allows for compensation of up to 256 ms or 2048 SONET frames. When all the members of a group have arrived, the members are interleaved to form the group data payload. The payload at this point consists of packets and idle frames. The packet processor would process this byte stream to extract Ethernet frames and

send them to the Ethernet MAC. MAC allows for loss-less traffic flow into the WAN[10] which is a very important feature for service providers.

Ethernet traffic may also be VLAN tagged by an edge router and one application may be to use VLANs to represent destination ports. Another application could use VLANs to segregate customer traffic. A VC group can then be allocated per destination port and can be sized to meet that destination's bandwidth requirement. There is no reverse flow control path through the WAN. Traffic that can't be forwarded to the Ethernet MACs must be discarded.

The SPI-4.2 bus can be used to connect the VC/GFP framer to Ethernet MACs as well as to Network Processors (NPUs) or Layer 2/3 switches. Separating the Ethernet Layer 2 or 3 data processing from the VC/GFP framer allows the their own solutions for traffic management and QOS in an FPGA.

The VC/LCAS design part could be run on a core-processor(micro blaze) . There are also certain operations like adding multiple members in one multiframe that would become difficult to manage with ASIC.

The VC/LCAS transmitter hardware has the responsibility of de-muxing the group data into the member SONET/SDH tributaries. This action needs to be synchronized with the control packet update and occurs on multiframe boundaries. The control packet may specify either an add or delete operation for each member of the group. The source hardware automatically formats the control packet and generates the pseudo-random GID (group ID bit) and CRC fields. The receiver hardware would be responsible for deskewing the members and producing a unified data stream. Several data structures are maintained in hardware. A scoreboard per group is maintained that is used to detect when all members have arrived. This event triggers the unloading of tributary data into the channel buffer. The deskew logic looks up the information it needs to reassemble the group in a control table. It is organized by multiframe and contains control words and sequence numbers. Software may also need access to this type of information so it should be dual ported. When all members have been unloaded from the SDRAM into the channel buffer the group is fully interleaved and data can be forwarded to the packet processor unit. Processing the LCAS control packet in hardware requires a framer to lock into the H4 MFI fields. Once in frame all the control packet bytes can be processed, prior to using the control packet the CRC must be checked. Failed CRC values result in the reuse of the previous control packet's state. In rare cases this will cause loss of a multiframe's worth of data. In addition to the member status table the hardware also monitors the GID bit. All members should have the same value per multiframe and an interrupt is generated when there is a mismatch. This feature of LCAS serves as a connectivity check to detect when members are not in the right group.

Conclusion

The next generation line card improve the transporting Ethernet traffic through SONET/SDH network. The card with VC/LCAS standard ,divide the task between hardware and software and provide reliable transport and extent the life of network for many years. These next generation card open up new opportunities for service provider on existing infrastructure and allows for higher utilization.

Due to flexible system these can be design for point to point Ethernet traffic and also can be used for other transporting scheme.

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