Comparative Analysis of Single Phase Multilevel AC/DC Converters

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***Abstract*—This paper presents a comparative study of single phase multilevel AC/DC converters. The simulation results are analyzed for different topologies with variations in load current and input power supply keeping the reference output voltage constant. In all the topologies only pulse width modulation (PWM) control scheme is used with hysteresis current controller. Simulations are carried out in MATLAB SIMULINK for fundamental frequency of 50 Hz for resistive loads only. Performance analysis shows that structure of these topologies have wide use in industrial applications as they have nearly unity power factor.**

***Keywords*— Pulse width modulation (PWM), improved power quality converters (IPQCs)**

I. Introduction

Traditional diode and thyristor based rectifiers used in power converter applications draw pulsed current from the input main which deteriorates the line voltage, produce radiated and electromagnetic interference leading to the poor efficiency. For single phase power applications, passive power filters, active one and two stage rectifiers are typical approaches used to achieve high power factor and low total harmonic distortion but they are bulky and heavy due to which there was a trade-off between their high efficiency, low cost and compactness. Active power factor correction techniques and active filters have been successfully researched and developed for power factor correction and current harmonics elimination, respectively. Power factor correction based on active current-shaping techniques has been presented in [1, 2] to improve the power quality of power converters. Among the high power factor converters, the boost type is the most popular [3, 4] for drawing a sinusoidal current from the AC mains with nearly unity power factor. For high power, the major concerns of conventional boost converters are inductor volume and weight, and losses on the power devices, which will affect converter cost, efficiency and power density. It has been shown in the literature that a single staged fly back converter can be operated as a single phase AC/DC converter with active power factor correction [5]. But the disadvantages of this conversion technique attributed mainly to the constant switching frequency and discontinuous nature of the current. In 1999 Active Input Current Shaper (AICS) was proposed [6] to turn a conventional Buck converter into a single stage AC/DC converter with high efficiency, fast transient response and low cost. Here, the disadvantages mainly attributed to the increased cost compared to the conventional topology due to the extra winding coupled to the buck's output inductor and the voltage magnitude higher than peak value, across the bulk capacitor. Even the two level converters did not prove themselves as improved quality converters (IPQCs) due to certain disadvantages as discussed in [7, 8]. To overcome the aforementioned difficulties faced by conventional conversion techniques, multilevel technology came into existence years back in 1975. The multilevel converters have drawn tremendous interest in the power industry [9]. Several factors are responsible for the research in this area and these converters have many advantages over the converters discussed earlier [10]. In this paper, only diode clamped and flying capacitor topologies are presented with MOSFETs used as switching devices.

II. Diode clamped Multilevel Converters

Fig. 1 shows a unidirectional three level diode clamped converter in which the dc bus comprises two capacitors C1 and C2. For dc bus voltage Vdc, the voltage across each MOSFET is Vdc/2. The voltages across two capacitors are balanced to Vdc/2 through a proportional controller. For modes of operation and control scheme in details see [11] although the control scheme which is used in all topologies is presented in later section. Fig. 2 shows a bidirectional three level diode clamped converter. This topology has six switches as compared to previous one (having four switches). This configuration also uses same control scheme.

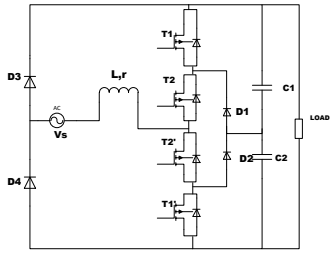


Figure 1. Power circuit of a three level diode clamp unidirectional converter.

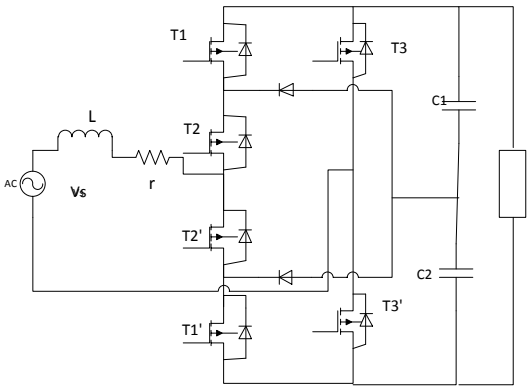


Figure 2. Power circuit of a bidirectional three level diode clamped converter.

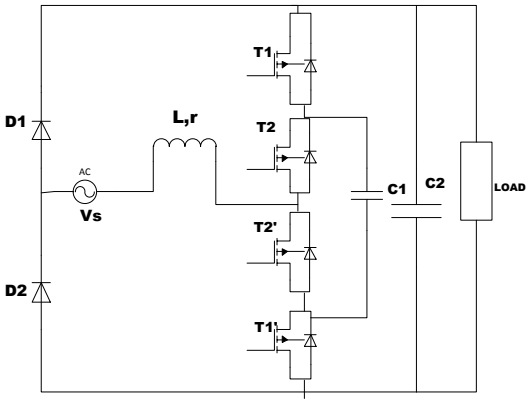


Figure 3. Power circuit of a unidirectional three level flying capacitor converter.

III. Flying Capacitor Multilevel converters

Fig. 3 shows an unidirectional three level converter. This configuration is exactly same as shown in figure except that clamped diodes are replaced by a capacitor. For details see [13]. The simulation results are shown in later section of this paper.

IV. Control Scheme

A control algorithm of the given topologies is proposed to achieve a constant DC-link voltage and to perform line current tracking with nearly unity power factor. The basic scheme is same in all cases except the PWM generator for generating the firing pulses for the switching devices. The generator is different for every topology depending upon mode of operation and has been discussed in details in papers. The control block diagram for three-level PWM modulation is shown in Fig. 4. A proportional integral (PI) voltage controller is employed in the outer low-bandwidth control system to maintain the constant DC-link voltage for balancing the real power between the mains and the DC load. Once the mains voltage or DC load changes, the real power between the load and mains is not sustained. The real power of the mains is changed by adjusting the current command to compensate the real power charged or discharged by the DC capacitor and to match the real power variation of the load. The current command is derived from the output of the voltage controller and the phase-locked loop circuit. The phase locked loop circuit generates a unit sinusoidal wave in phase with the mains voltage. The line current is compared with the line current command, i_s*. The hysteresis current controller is used to track the line current command.

V. MATLAB Simulations

Simulations of the converter topologies are conducted for various modes of operation using MATLAB. Single phase AC source of fundamental frequency 50 Hz is used. As mentioned earlier, the control scheme used is PWM with hysteresis current controller for current control loop and PI controller for balancing the output DC voltage. The simulation parameters are as follows:

Vs = Input single phase voltage magnitude (rms).

Is = Input source current.

Vdc = Magnitude of DC output voltage.

Vab = Voltage levels on AC input side.

R = Load resistance.

L = Inductance of single phase supply.

r = Resistance of single phase supply.

VI. Results and Discussion

The results of simulations for topologies discussed earlier are shown and discussed in this section. First results are shown for Fig. 1 and so on in increasing order of topologies discussed. The parameters used for simulations are as Vs = 110V and 50V, Vdc = 200V, r = 0.4 ohm, L = 5mH and R = 50 Ohms, 100 Ohms and 200 Ohms. The results shown in Fig. 4 are for topology shown in Fig. 1 for 110V supply and for all resistive loads. Fig. 5 shows the simulation results of same topology but for input supply of Vs = 50V. The results of Vab shows that level of voltages on the AC side has decreased to two levels only. Input source current has increased significantly. This has a reason behind it. To generate a three-level voltage waveform on the AC side of the converter, the mains voltage must be less than the DC bus voltage and greater than half of the DC bus voltage. Two operating regions

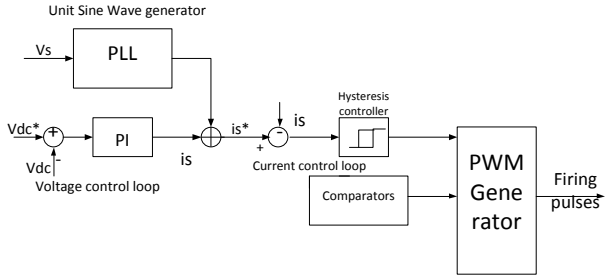
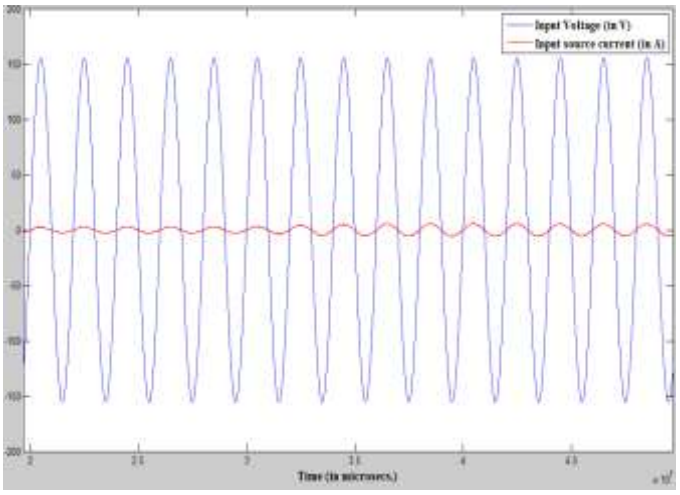


Figure 4. Control block diagram.



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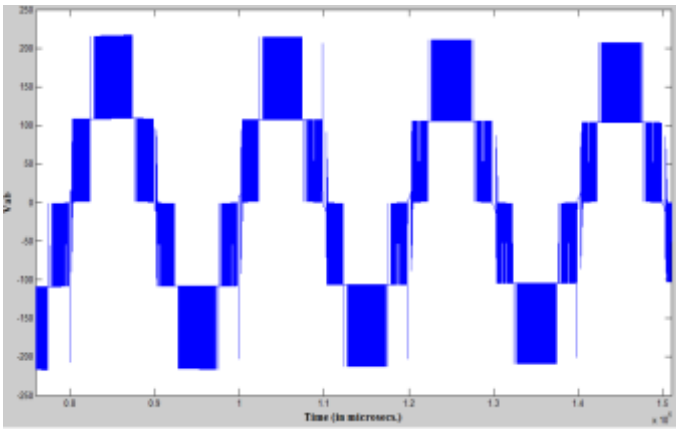

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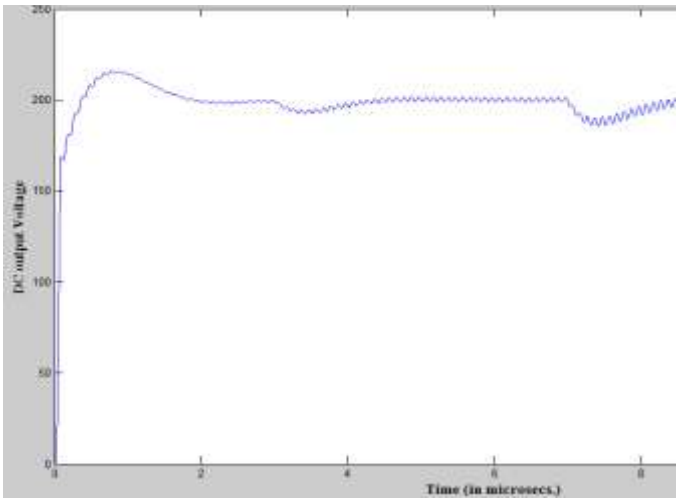

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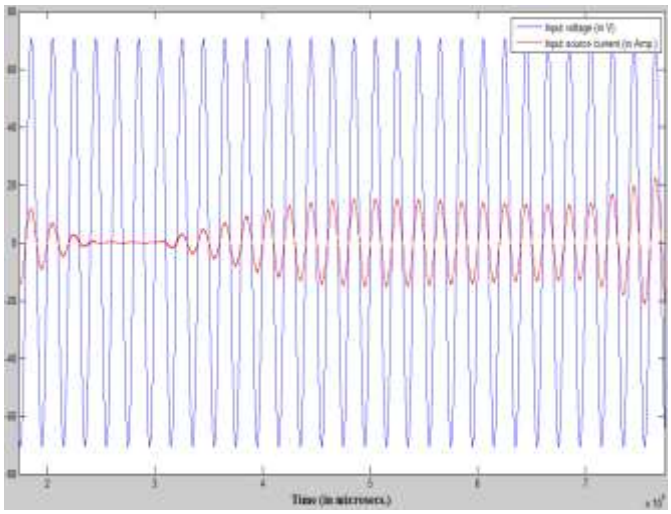
Figure 5. Simulation results of topology shown in Fig. 1 showing (a) Input voltage and source current (b) Vab (c) DC output voltage.

of mains voltage during one cycle of mains frequency are defined and shown in fig. 7.



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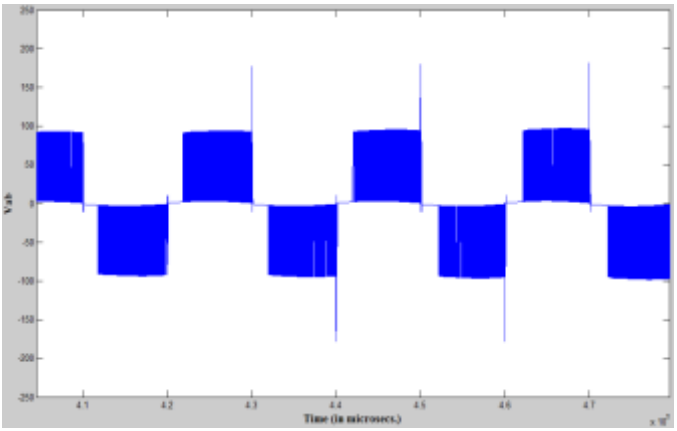

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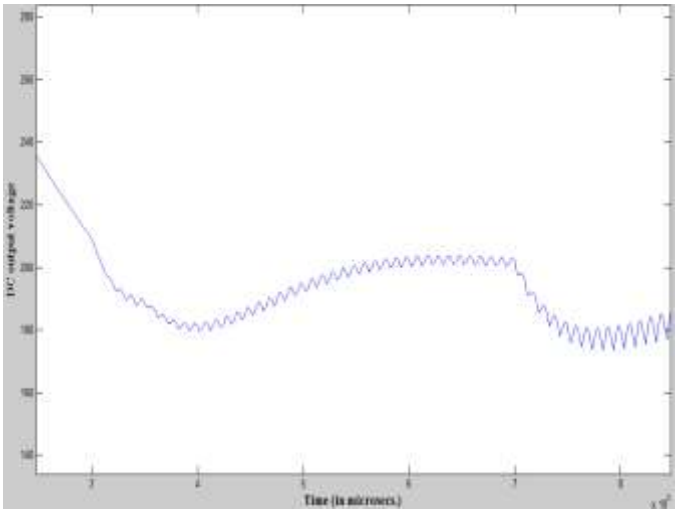

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Figure 6. Simulation results for input supply of 50V showing (a) Input voltage and source current (b) Vab (c) DC output voltage.

In the first region, the instantaneous mains voltage is greater than –Vdc/2 and less than Vdc/2. Voltage levels 0 (low

voltage level) and Vdc/2 (high voltage level) are generated on voltage Vab in the positive mains voltage to control the line current. During the negative mains voltage, voltage levels -Vdc/2 (low voltage level) and 0 (high voltage level) are selected to control the line current. In the second region, the absolute value of the mains voltage is less than the DC bus voltage Vdc but greater than half of the DC bus voltage Vdc/2. Voltage levels Vdc and Vdc/2 (or -Vdc and -Vdc/2) are generated during the positive (or negative) half-cycle of the mains voltage to control the line current. So, when input mains supply is reduced below the Vdc/2 value (keeping reference Vdc value constant) only region 1 is left for the operation of converter and hence the number of levels on AC side gets reduced. Thus, two such values are chosen for showing the difference. If the magnitude of Vs is reduced even below 50V, the results would be distorted more.

Note: In all the results shown the x-axis is time in microseconds. The waveforms in blue are voltages in volts and that in red is source current in amperes.

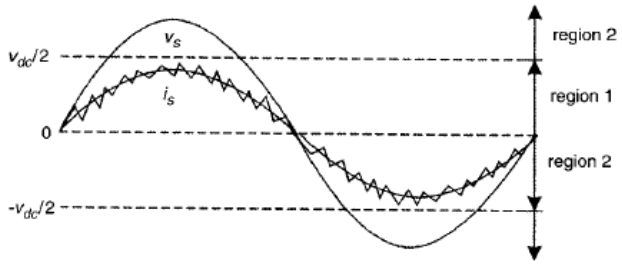
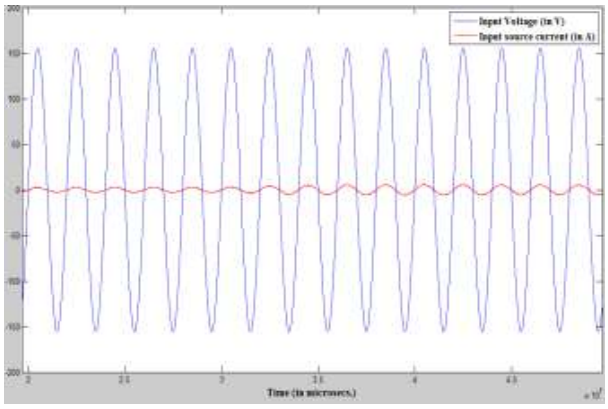


Figure 7. Operating regions of a three level converter.



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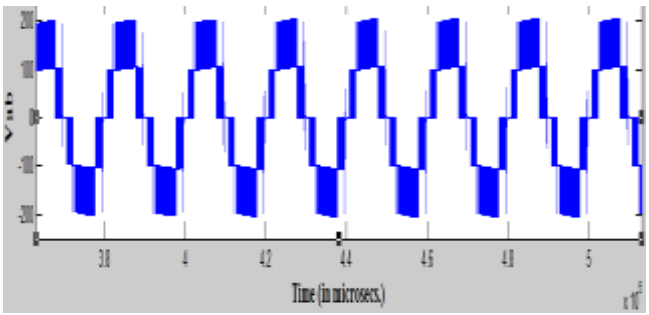

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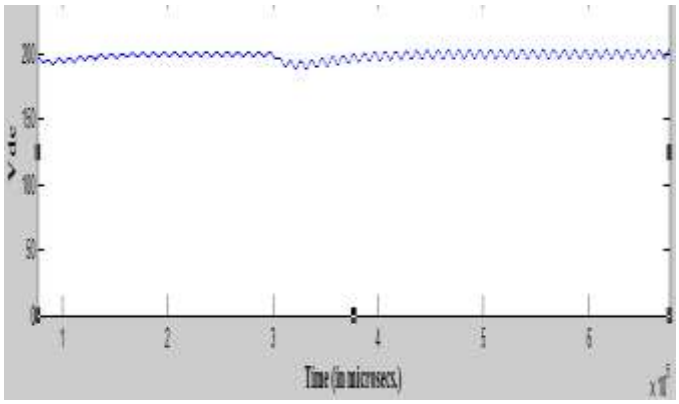

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Figure 8. Simulation results for topology shown in Fig. 2 for 110V input voltage showing (a) input voltage and source current (b) Vab (c) Vdc.

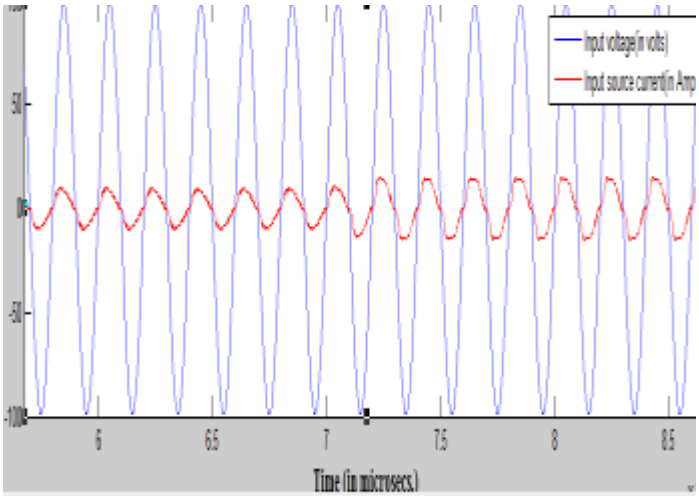
Fig. 8 shows the simulation results of topology shown in Fig. 2 for input supply of 110V. DC output voltage is shown for load of 100 Ohms and 50 Ohms respectively in result window. Fig. 9 shows the simulation results for the topology shown in Fig. 3 for input voltage Vs of 70V. We can see that number of levels on AC input side reduce to two for a three level converter and source current waveform gets distorted as load current increases.

VII. Conclusion

We can see that input voltage and input source current are in phase with each other and current waveform is nearly sinusoidal. It says that power factor is nearly unity and very less harmonics are present in current which increases the efficiency at output receiving end. After having seen simulation results of all aforementioned topologies with varying load and varying input voltage supply, we can conclude the following results with certain justifications.

- Firstly, the number of voltage levels decrease on AC input side with decreasing input mains voltage keeping the reference Vdc constant. The reason has already been discussed.
- Secondly, the ripples in the DC output voltage increase with increasing load current because of the unbalance of the voltages across the capacitors of DC bus. This unbalance increases as charging and discharging of capacitors takes place at different rate.
- Thirdly, a three level converter can produce the maximum DC output voltage of magnitude twice the peak value of input mains voltage due to the fixed capacitors on the DC bus link. Thus, the output DC voltage is not regulated and maintained at reference voltage as is clear from the simulation results.

Besides these conclusions the multilevel converters promise a bright future especially in the power industry if the appropriate parameters are chosen.



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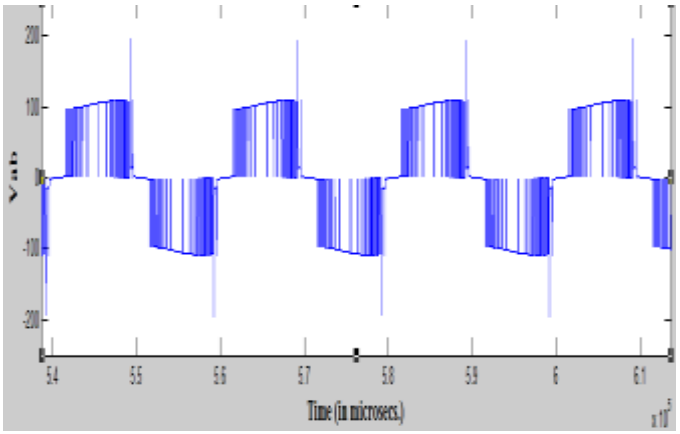

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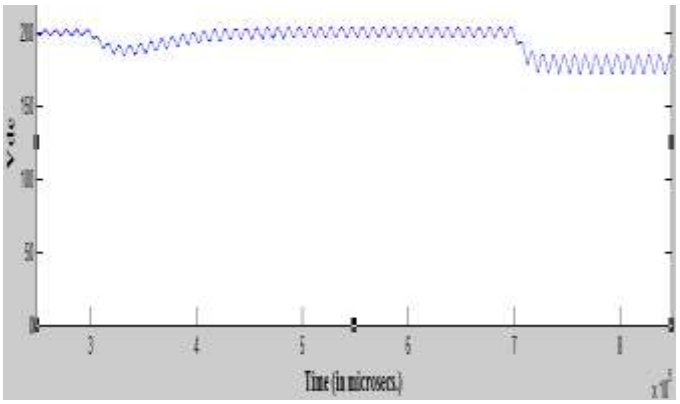

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Figure 9. Simulation results for topology shown in Fig. 3 for Vs = 70V showing (a) input voltage and source current (b) Vab (c) Vdc.

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