Two DDCC Based Cascadable Voltage-Mode First-Order All-Pass Filters

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***Abstract*—In this paper, four new voltage-mode first-order all pass filters are proposed. Each circuit employs two differential difference current conveyors (DDCC) and two passive components with no matching condition. The proposed circuits offer high-input and low-output impedance, low active and passive sensitivities, which is a desirable feature for the voltage-mode systems. Non-ideal analysis and parasitic effect study is also performed. The theoretical results are verified by SPICE simulation.**

Keywords— All-pass filter, analog circuits, current conveyor, signal processing.

I. INTRODUCTION

First-order all-pass filters are widely used in analog signal processing to correct the phase shift without changing the amplitude of the applied signal over the frequency range. All-pass filters made from operational amplifier (op-amp) often suffer from limited gain-bandwidth product and slew-rate [1-2].

Recently, current conveyor have been used in implementation of either a current mode or voltage mode filters because of their excellent features such as wide bandwidth, simple circuitry, wider dynamic range, greater linearity, low power consumption as compared to op-amp based voltage-mode filters. Considering these advantages of current mode circuits recently, several voltage mode, all pass filters using various active components have been reported [2-26]. Unfortunately the careful literature review of the previously reported circuits suffer from the following limitations:

- use of excessive passive components. [3-8, 10-13, 15-17, 19]
- use of floating capacitor, which is not desirable for IC implementation. [3, 5, 7-8, 11,19]
- requirement of element-matching constraints. [3-8, 10-13, 15, 17, 19]
- Low-input impedance. [4-9, 11, 14, 18, 20-22]

Although the proposed filters in [20-21] employ a single DDCC, one grounded capacitor and one floating resistor. Similarly a single DDCC based all-pass filter with a floating capacitor and grounded resistor was presented in [22]. Such circuits aim is to realize first-order all-pass filter using optimum number of active and passive components rather than offering high-input and/or low-output impedance. The recently reported circuits in [23-25] realize first-order all-pass filters using single FDCCII with grounded components. However it may be noted that a single FDCCII requires more number of transistors than two DDCC together.

The aim of this paper is to propose cascadable voltage-mode (VM) first-order all-pass filters by employing two DDCCs, a resistor and a grounded capacitor. The proposed filters offer high-input impedance and low-output impedance. It may be noted that the input impedance should be larger in comparison to the output impedance to avoid loading problem while cascading such circuits to form larger system. Also, the two component based all-pass filter circuits are benefit from the no matching constraint as compared to three or more component based circuits (exceptions are possible if pole and frequency determining components are same). Though a very recently reported filter circuit in [26] employ equal number of active and passive component as the proposed circuit employed but it cannot enjoy the low output impedance at the output terminal. Non-ideal gain and parasitic effects of the DDCCs on the transfer functions of the proposed filters are also investigated.

II. THE PROPOSED CIRCUIT

The DDCC whose symbol is shown in Figure 1 [27], is a five terminal active element with the following defining equation

$$V_X = V_{Y1} - V_{Y2} + V_{Y3}; \quad I_{Y1} = I_{Y2} = I_{Y3} = 0; \quad I_X = I_{Z+} \qquad (1)$$

where the suffixes refer to the respective terminals. The voltage at X-terminal follows the voltage difference and addition of terminal Y_1, Y_2, Y_3. The current at terminal Z follow the current at terminal X. The DDCC is characterized by high input impedance at the Y_1, Y_2, and Y_3 terminals, high output impedance at the Z+ terminal and low impedance at the X terminal. DDCC is a useful and versatile active element which

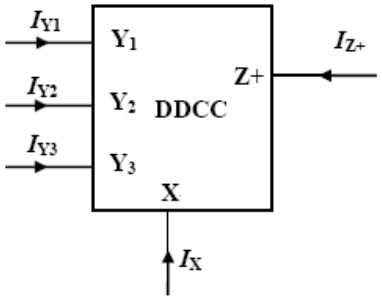
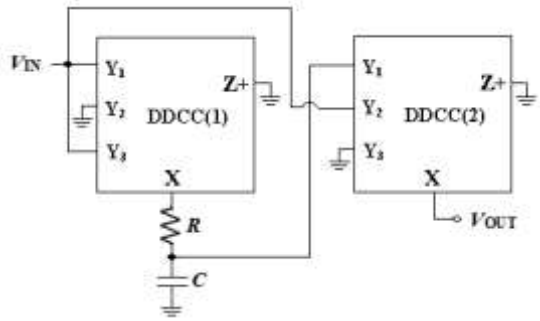
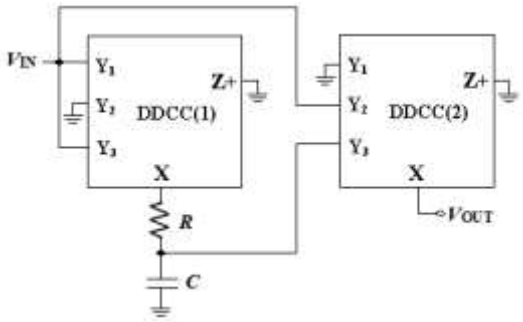


Figure 1. Symbol of DDCC.



(*a*)



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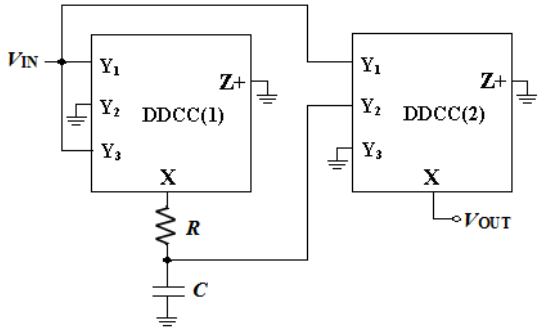

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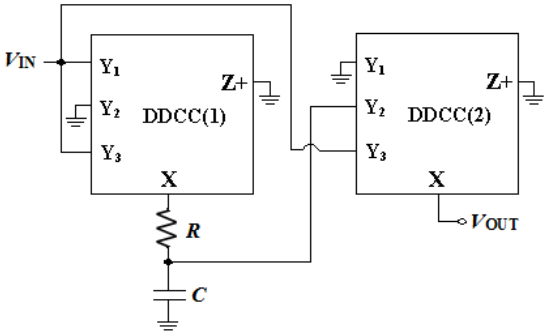

(*d*)

Figure 2. Proposed VM first order all-pass filters (*a*) Circuit-1; (*b*) Circuit-2; (*c*) Circuit-3; and (*d*) Circuit-4.

has found several applications for analog signal processing [20-22, 28-31].

The proposed VM first order all-pass filters employing two DDCCs, one grounded capacitor and one resistor are shown in Figure 2. Routine analysis of the circuits, gives the following transfer function

$$\frac{V_{OUT}}{V_{IN}} = -\left(\frac{s-(1/CR)}{s+(1/CR)}\right) \qquad (2)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{s-(1/CR)}{s+(1/CR)} \qquad (3)$$

Equation (2) is the transfer function of circuit-1 and -2 with the frequency dependent phase shift Φ = -2 $\tan^{-1}(\omega RC)$, whereas (3) is the transfer function of circuit-3 and -4 with the frequency dependent phase shift $\Phi = 180^0$-2 $\tan^{-1}(\omega RC)$. The salient features of the proposed circuits are high input and low output impedance, use of minimum number of passive components and using grounded capacitor that is attractive for integrated circuit implementation.

It is also worth mentioning that four additional new circuits can further be obtained from the proposed circuits by interchanging the resistor (R) with a capacitor (C). However these circuits would employ a capacitor at X terminal, thus degrading high frequency operation.

III. NON-IDEAL ANALYSIS AND PARASITIC EFFECT

A. *Non-ideal analysis*

Taking the non-idealities of the DDCC into account, the relationship of the terminal voltages and current of DDCC can be rewritten as

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_{k1} & \alpha_{k2} & \alpha_{k3} & 0 & 0 \\ 0 & 0 & 0 & \beta_{k1} & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_Z \end{bmatrix} \tag{4}$$

where α_{k1}, α_{k2}, α_{k3} (k = 1, 2) is the voltage transfer gain from Y_1, Y_2 and Y_3 to the X terminal and β_{k1} is the current transfer gain from X terminal to the Z+ terminal of the k-th DDCC respectively. These transfer gains differ from unity by the voltage and current tracking errors of the DDCC. More specifically, $\alpha_{k1} = (1 - \varepsilon_{k1})$, $\alpha_{k2}=(1 - \varepsilon_{k2})$, $\alpha_{k3} = (1 - \varepsilon_{k3})$, and $\beta_{k1} = (1 - \delta_{k1})$ where, ε_k is the voltage transfer error (tracking error) of the k-th DDCC and δ_k is the current transfer error (tracking error) of the k-th DDCC. Reanalysis of the circuits in Figure 2 using this description yields the following voltage transfer functions

$$\text{Circuit-1: } \frac{V_{OUT}}{V_{IN}} = -\alpha_{22}\left(\frac{s + \frac{\alpha_{22} - \alpha_{21}(\alpha_{11} + \alpha_{13})}{CR\alpha_{22}}}{s + \frac{1}{CR}}\right) \tag{5}$$

$$\text{Circuit-2: } \frac{V_{OUT}}{V_{IN}} = -\alpha_{22}\left(\frac{s + \frac{\alpha_{22} - \alpha_{23}(\alpha_{11} + \alpha_{13})}{CR\alpha_{22}}}{s + \frac{1}{CR}}\right) \tag{6}$$

$$\text{Circuit-3: } \frac{V_{OUT}}{V_{IN}} = \alpha_{21}\left(\frac{s + \frac{\alpha_{21} - \alpha_{22}(\alpha_{11} + \alpha_{13})}{CR\alpha_{21}}}{s + \frac{1}{CR}}\right) \tag{7}$$

$$\text{Circuit-4: } \frac{V_{OUT}}{V_{IN}} = \alpha_{23}\left(\frac{s + \frac{\alpha_{23} - \alpha_{22}(\alpha_{11} + \alpha_{13})}{CR\alpha_{23}}}{s + \frac{1}{CR}}\right) \tag{8}$$

From (5) – (8), the pole frequency (ω_o) and gain (H) sensitivity to the non-idealities as well as passive components is analyzed and tabulated in Table I.

TABLE I. SENSITIVITY FIGURES

Sensitivities	Circuits			
	-1	-2	-3	-4
$S_{R,C}^{\omega_0}$	-1	-1	-1	-1
$S_{\alpha_{11},\alpha_{12},\alpha_{13},\alpha_{21},\alpha_{22},\alpha_{23},\beta_{11},\beta_{21}}^{\omega_0}$	0	0	0	0
$S_{\alpha_{21}}^{H}$	0	0	1	0
$S_{\alpha_{22}}^{H}$	1	1	0	0
$S_{\alpha_{23}}^{H}$	0	0	0	1
$S_{\alpha_{11},\alpha_{12},\alpha_{13},\beta_{11},\beta_{21},R,C}^{H}$	0	0	0	0

Table I ensures a good sensitivity performance of the proposed circuits.

B. *Parastic effects*

To account for parasitic element, the port X exhibits of low value parasitic serial resistance R_X, the ports Y_1, Y_2 and Y_3 exhibit of high value parasitic resistance R_Y in parallel with low value capacitor C_Y and the port Z exhibit of high value parasitic resistance R_Z in parallel with low value capacitance C_Z [32]. All the proposed circuits employs resistor at the X terminal of the DDCC, hence the involvement of R_X is important, beside port Y and Port Z parasitic. A reanalysis of the four circuits, yield the transfer function as

$$\frac{V_{OUT}}{V_{IN}} = k\left(\frac{s - \frac{1}{C(R + R_X)}}{s + \frac{1}{C(R + R_X)}}\right) \tag{9}$$

where k = +1 for circuit-1 and -2, and k = -1 for circuit-3 and -4.

From (9), the proposed circuit would exhibit a slight deviation in the pole frequency from the designed value but the deviation is small for an integrated DDCC.

IV. SIMULATION RESULTS

Simulation program with integrated circuit emphasis (SPICE) were carried out to demonstrate the performance of the proposed circuits using 0.5 μm CMOS parameters from MOSIS. The CMOS implementation of DDCC is shown in Figure 3 [29], which was modified by eliminating the unused Z+ output terminal from the original DDCC, since it is

grounded in the proposed circuits (Figure 2). The aspect ratios of the CMOS transistors of the DDCC are listed in Table II. DC supply voltages of ±2 V and biasing voltage of V_{BB} = -1.15 V were used . The circuit of Figure 2 was designed with R = 10 KΩ, and C = 1 pF. The gain and phase responses are shown in Figure 4, where a pole frequency of 15.88 MHz is obtained. This is close to the theoretical value of 15.91 MHz. The time domain responses of the proposed circuit-I are shown in Figure 5. The Fourier spectrum of input signal and output signal are shown in Figure 6. Next the signal amplitude is varied from 1mV to 500mV and the Total haromic distrortion (THD) curve is plotted at a frequency of 15.91 MHz is shown in Figure 7.

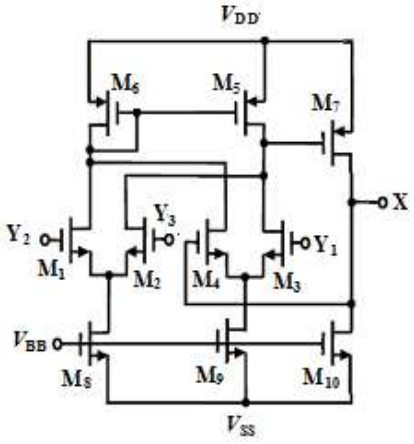

Figure 3. CMOS implementation of DDCC.

Table II. ASPECT RATIOS OF THE TRANSISTORS FOR THE FIGURE 3.

Transistors	W(μm)	L(μm)
M_1, M_2, M_3, M_4	0.8	0.5
M_5, M_6	4	0.5
M_7	10	0.5
M_8, M_9	14.4	0.5
M_{10}	45	0.5

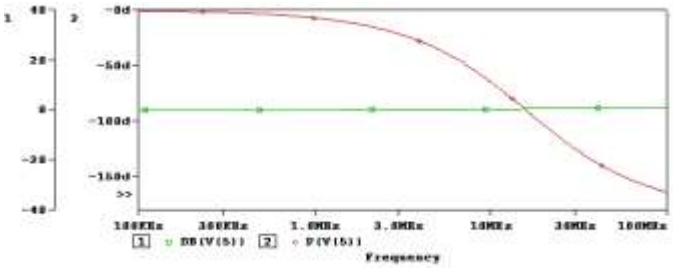

Figure 4. Simulated Gain and Phase response for circuit-1.

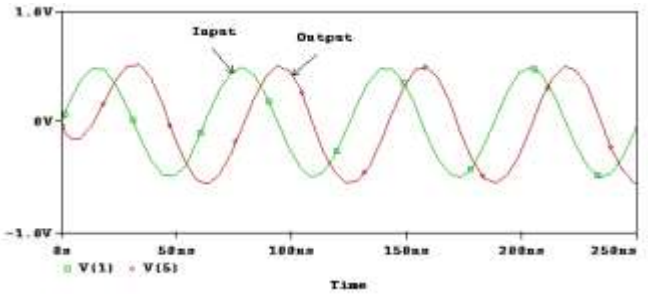

Figure 5. Time domain Input-output responses of Circuit-1

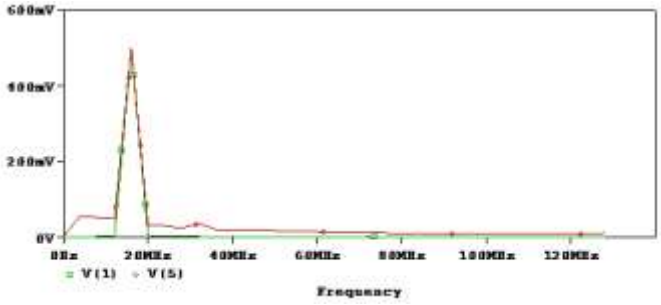

Figure 6. Fourier spectrum of the input and output signal.

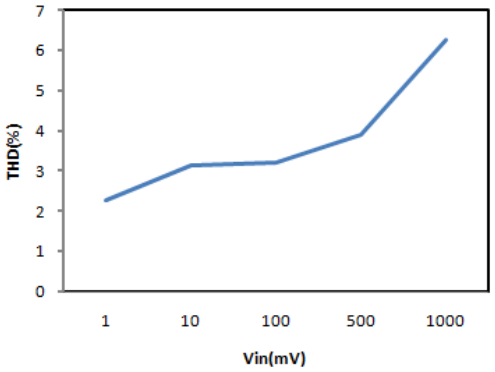

Figure 7. THD Variation at output with signal amplitude at 15.91 MHz.

V. CONCLUSION

In this paper, four new voltage-mode first-order all-pass filters employing two DDCCs are proposed. Each circuit posses high-input impedance and low-output impedance and uses a grounded capacitor, which is suitable for Integrated circuit implementation[33]. The SPICE simulation results of the proposed circuits depict good frequency performance over the existing circuits.

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