Voltage Controlled Current Conveyor and its Application

Susheel Sharma[#1] & Rockey Gupta[#2]

[#]Department of Physics and Electronics
University of Jammu
Jammu-180006, India
[1]susheelksharma@gmail.com
[2]rockeygupta@gmail.com

Abstract— **In this paper a voltage controlled current conveyor is presented wherein the intrinsic transresistance is controlled by a voltage variable current source which is realized using floating-gate MOSFETs. The resultant conveyor has been used to implement an impedance converter which is further used as inductance simulator. The characteristics of the conveyor and inductance simulation have been obtained through PSpice simulations carried out using level 3 parameters of 0.5 µm CMOS technology with supply voltage of ± 0.75 V. The simulation results are found to be in conformity with the mathematical analysis.**

Keywords- current controlled current conveyor; current source; inductance simulation

I. INTRODUCTION

The second generation current conveyor (CCII) has proved to be a versatile building block being employed in a variety of analog circuits. This device suffers from shortcomings like large voltage tracking error from terminal Y to terminal X due to parasitic resistance at terminal X and the lack of electronic tunability. In 1996, Fabre proposed a BJT based second generation current controlled conveyor (CCCII) by utilizing the parasitic intrinsic transresistance at port X which can be tuned electronically by adjusting the bias current [1-8]. Though BJT has advantage of low noise and high operating frequency, but not compatible with CMOS VLSI technology for integration.

In this paper, we have presented a voltage controlled current conveyor (VCCCII) where the intrinsic resistance of conventional CCCII is controlled by a voltage variable current source realized using floating-gate MOSFETs. The characteristics of the modified current conveyor are studied and it has been further employed for implementing an impedance converter which realizes a tunable inductance simulator.

II. VOLTAGE CONTROLLED CURRENT CONVEYOR

The voltage controlled current conveyor (VCCCII) is a modified form of CCCII which is basically a three port device shown in Fig. 1 and characterized by the following matrix equation.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

where R_x is a parasitic resistor present at terminal X and dependents inversely on the bias current(I_B).

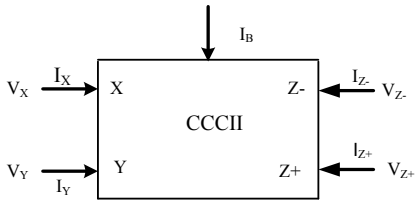

Figure 1. Block diagram of CCCII.

A. *Voltage controlled current source*

The bias current in CCCII is generated by a voltage controlled current source (VCCS) as shown in Fig. 2. The circuit of VCCS is based on floating-gate MOSFETs (FGMOS) where the output current is controlled by the bias voltage (V_{bias}). Transistors M1 and M2 form the basic FGMOS CM where C_1 is grounded [9-11]. M3 acts as an input current source for M1 which has been suitably biased to feed a variable input current. Transistors M5-M7 form an arrangement to provide a variable bias to M3. It has been achieved by connecting the gate of M3 to the drain of M6 that acts as a constant current source and provides a variable bias point. The output current is taken from M2 and applied as input bias current to translinear CCCII. The output current of FGMOS based VCCS depends on C_2/C_1 ratio and V_{bias} and is given as:

$$I_{out} = \frac{\beta_2}{2}\left[\left(\frac{C_2/C_1}{1+C_2/C_1}\right)V_{bias} - V_T\right]^2 \quad (1)$$

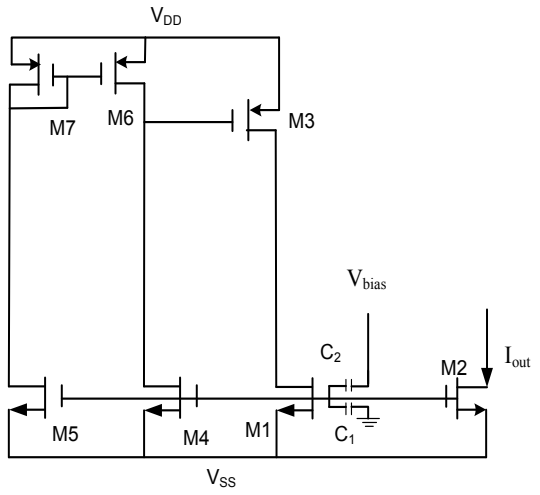

Figure 2. Voltage controlled current source.

This circuit has been simulated by using level 3 PSpice parameters of 0.5 µm technology with supply voltages of ± 0.75 V by choosing *W/L* ratios for M1 and M2 as 0.5µm/1µm and 100µm/0.5µm for M3, 50µm/1µm for M4 and M5, 50µm/0.5µm for M6 and M7. The variation of output current due to different bias voltages is shown in Fig. 3. The current source has output resistance of 5.56 MΩ and dissipates 2.31mW power.

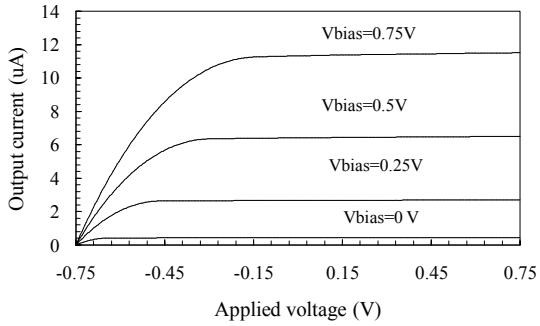

Figure 3. Output characteristics of VCCS.

B. CMOS implementation of VCCCII

The CMOS implementation of the proposed voltage controlled current conveyor (VCCCII+) is shown in Fig. 4 which has been obtained by using VCCS of Fig. 2 along with the conventional structure of CCCII+ [1, 2]. The VCCS provides different biasing current to CCCII+, therby resulting in different values of intrinsic resistance present at port X.

In Fig. 4 transistors M1-M7 & M10-M11 form a FGMOS based voltage controlled current source which supplies bias current to the translinear loop formed by M19- M22. The rest of the transistors form current mirrors for biasing purpose.

This circuit has been simulated by using level 3 PSpice parameters of 0.5 µm technology with supply voltages of ± 0.75 V by choosing *W/L* ratio of 200µm/0.5µm for M16-M18, M12-M13, M22 & M19 and 400µm/0.5µm for M8-M9, M14-M15, M20 & M21. The transistors M10 and M11 are used to invert the current from voltage controlled current source and have *W/L* ratios as 50µm/0.5µm. Fig. 5 shows the voltage transfer characteristic of the VCCCII+. The voltage transfer ratio has been found to be 0.998 with a bandwidth 152.27 MHz as shown in Fig. 6. The input resistance at port Y is found to be 3.33 MΩ and output resistance at port X is 1.2 kΩ. The current transfer ratio has been found to be unity. The bandwidth for current transfer is found to be 120 MHz as shown in Fig. 8. The input resistance at port X is found to be 1.22kΩ and output resistance at port Z is 4.49 MΩ. The variation of intrinsic resistance (R_x) at port X is shown as a function of bias voltage in Fig. 9. It is found that R_x varies from 31kΩ to 1.2 kΩ as the bias voltage varies from 0V to 0.75V.

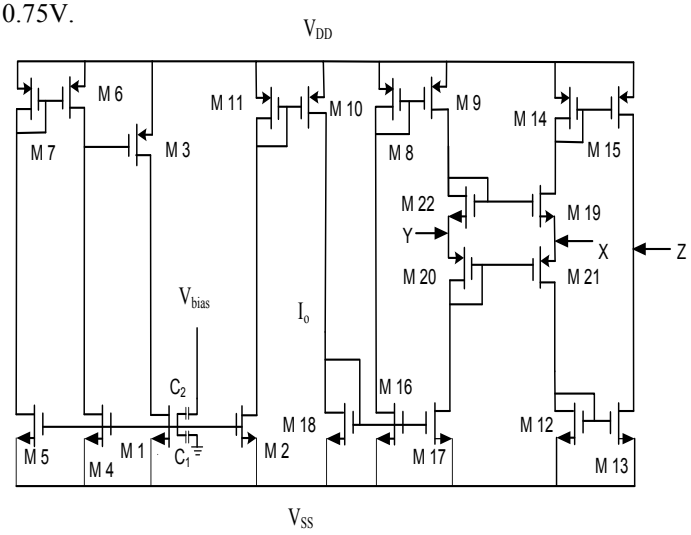

Figure 4. Circuit of VCCCII+.

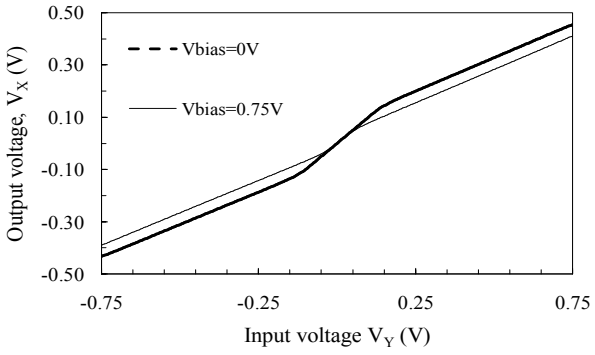

Figure 5. Voltage transfer characteristics of VCCCII.

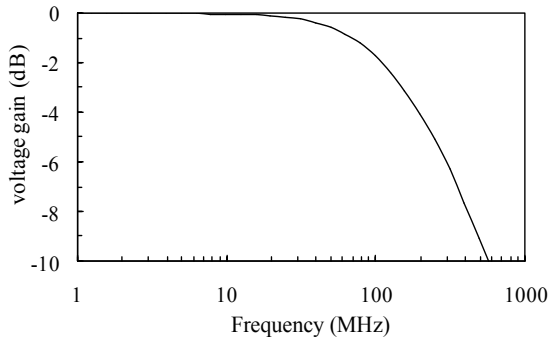

Figure 6. Frequency response of voltage transfer of VCCCII.

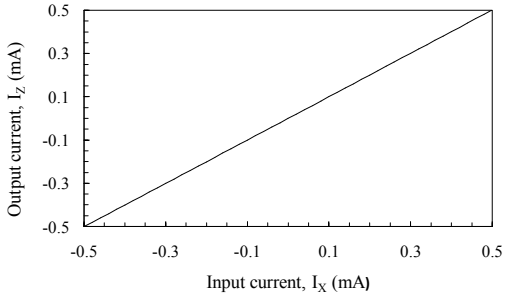

Figure 7. Current transfer characteristics of VCCCII.

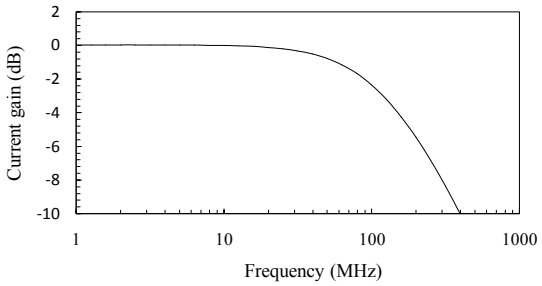

Figure 8. Frequency response of current transfer of VCCCII.

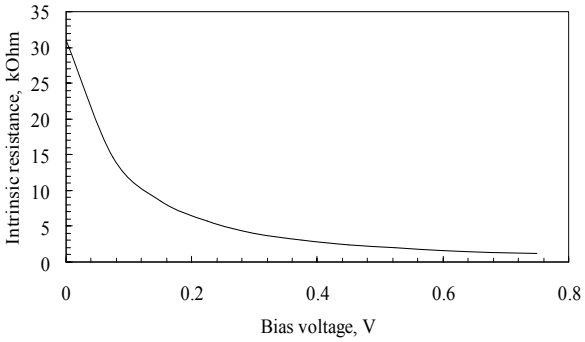

Figure 9. Variation of intrinsic resistance with bias voltage.

A negative polarity voltage controlled current conveyor is obtained by inverting the output current of VCCCII+ using a bipolar current mirror as depicted in Fig. 10. The voltage transfer characteristics are found to be similar to that of VCCCII+. The current transfer characteristic is shown in Fig. 11.

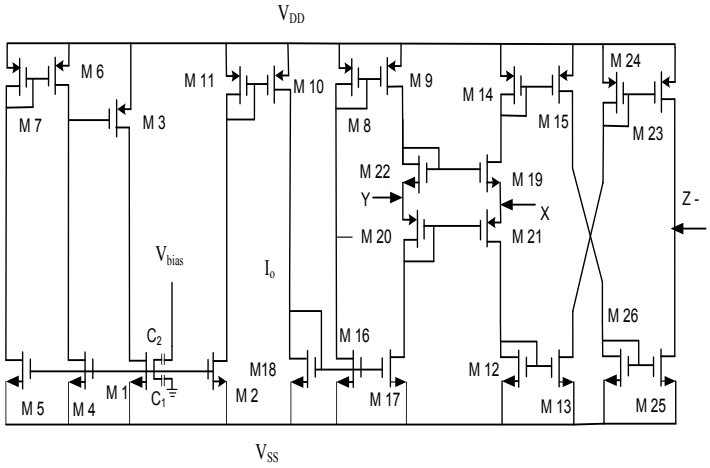

Figure 10. Circuit of VCCCII-.

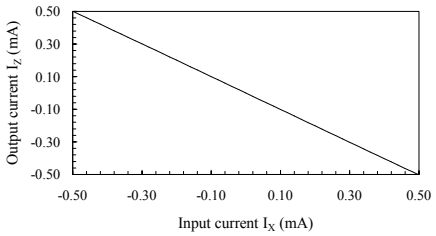

Figure 11. Current transfer characteristics of VCCCII-.

III. IMPEDANCE CONVERTER

Impedance converters are often used to simulate inductance using capacitance and to obtain higher values of capacitance from low capacitor value available on chip. Inductance simulation has attracted considerable interest in the implementation of active inductorless filters on the chip, where the use of physical inductors is prohibited due to their size and weight except at high frequencies [12-15]. Impedance converter is realized by connecting a VCCCII+ and VCCCII- as shown in Fig.12. This is equivalent to connecting a positive and a negative transconductor back to back [12, 13].

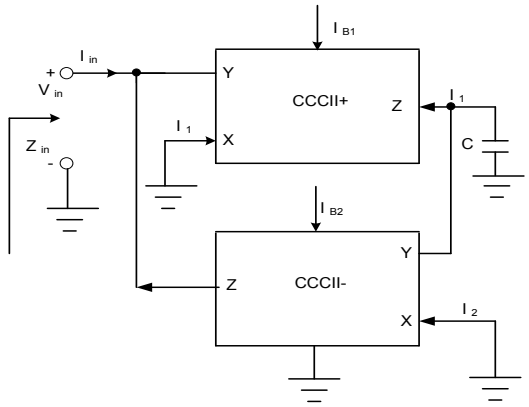

Figure 12. Circuit of impedance converter.

The analysis of Fig. 12 shows that the input impedance is inductive in nature and is given by:

$$Zin = \frac{V_{in}}{I_{in}} = sRx_1Rx_2C \quad (2)$$

which gives simulated inductance given by:

$$L_{simulated} = R_{x1}R_{x2}C \quad (3)$$

Therefore by terminating the output port of VCCCII+ with a grounded capacitor, we can obtain a grounded inductor. The inductive nature of the input impedance is shown in Fig. 13. The different inductance values are simulated by using different bias voltages with C=1nf as shown in Fig. 14 with respective phase shift in Fig.15. It can be concluded that usable frequency range of simulated inductance decreases with higher value of simulated inductance.

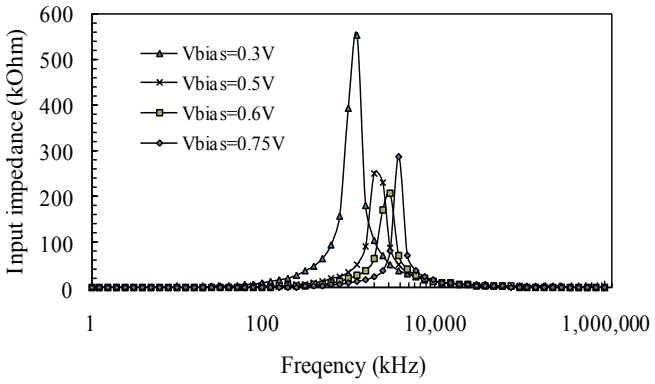

Figure 13. Input impedance of impedance converter.

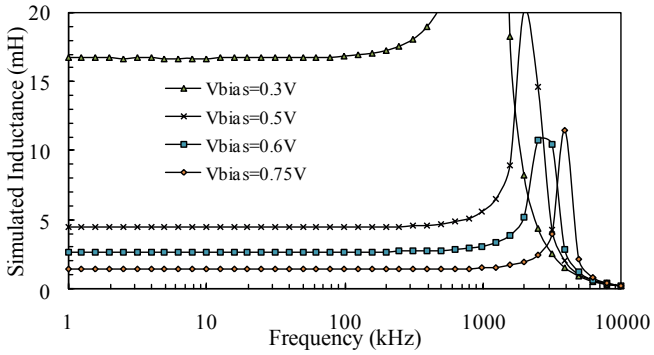

Figure 14. Voltage variable inductance simulation.

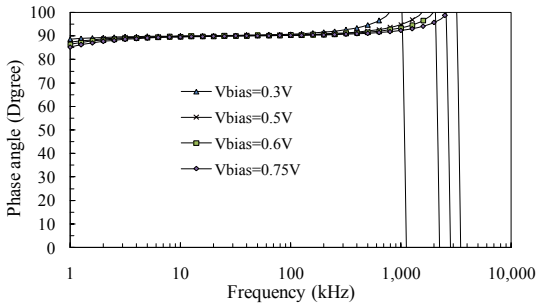

Figure 15. Phase response of different inductance simulations.

The simulation results have been found to be in good agreement with theoretical predictions as shown in following table 1.

TABLE I. COMPARISON OF THEORETICAL AND SIMULATED INDUCTANCE

V_{bias}	$L_{theoretical}$	$L_{simulated}$
0 V	961 mH	958 mH
0.15 V	74.24 mH	73.5 mH
0.3 V	16.84 mH	16.7 mH
0.5 V	4.51 mH	4.48 mH
0.6 V	2.73 mH	2.71 mH
0.75 V	1.46 mH	1.45 mH

IV. CONCLUSIONS

In this paper, we have presented the modified form of current controlled current conveyor using a voltage controlled current source. The resultant voltage controlled current conveyor has been characterized and employed in the realization of impedance converter which can simulate a wide range of inductance depending on the value of the bias voltage. The circuit behavior has been studied using PSpice simulations which have been found in good agreement with theoretical results. The tunable inductance can be used to realize inductorless active filters suitable for VLSI integration.

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