# Low Power Low Voltage CMOS Mixed Signal Operational Amplifier

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**Abstract:**

***This paper presents a new methodology for design of high speed CMOS operational amplifier in Sub-micron region. The op-amp uses a compensation technique which increases the unity gain frequency and phase margin simultaneously. The CMOS op-amp presented in this paper works on 1.5V designed in 65nm standard CMOS technology. It exhibits 86dB DC gain. With load of 5pF, the unity gain frequency and phase margin are 34MHz and 84$^o$ respectively. The op-amp is fairly small and slew rate is more than other low power low voltage op-amps reported.***

***Keywords: OTA, deep sub-micron, Advanced Design System (ADS), Compensation technique***

## 1. INTRODUCTION

Silicon technology continues to scale down to ever smaller sizes to reach the market need to include more and more transistors on chip and faster processing of microprocessor. While such scaling is beneficial to digital CMOS circuit behaviour, analog devices are not always benefited by smaller device sizes and lowered supply voltage. As the transistor lengths decrease in size, the effect of channel modulation has a greater impact and drain current increases speedily with a larger $V_{DS}$. To develop efficient electronic equipment the semiconductor industry has pushed the circuit designers towards low voltage power supply and low power consumption of circuits [1]. New smaller size process technologies offer opportunities to designer to operate at higher frequencies consuming less power, but for analog circuits, this fact partially applies since it is often the case that additional current is needed to keep the same performance when the power supply voltage is decreased. Power dissipation in a circuit can be reduced by reducing either supply voltage or total current in the circuit or by reducing the both. As the input current is lowered though power dissipation is reduced, dynamic range is degraded. As the supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the voltage headroom available [2].

With developments in deep sub-micron CMOS processes, the available dynamic range in Operational Amplifiers (op-amps) is reduced due to lower power supply voltages [3]. This loss in dynamic range tightens the noise budget. Therefore, a larger load capacitor must be used to reduce the circuit noise, and hence increase the Signal-to-Noise Ratio (SNR), which in turn decreases the bandwidth of the amplifier [4]. With ever increasing data rates, many mixed-signal applications require op-amps having less settling time. Therefore, op-amp design has become exceedingly difficult for broadband circuits while maintaining adequate SNR performance. Techniques for increasing the bandwidth of CMOS Op-Amps are needed to accommodate high speed operation with low noise performance. Thus, typical analog design techniques are needed in order to face the above issues.

This paper is organized as follows. In Section 2, a compensation method for high speed CMOS Op-Amps is described. The design of an Op-Amp based on this approach is explained in Section 3. Simulation results are described in Section 4. Finally, some conclusions are offered in Section 5.

## 2. HIGH SPEED CMOS OP-AMP

CMOS operational amplifier is designed usually by using Operational Trans-conductance Amplifier (OTA) followed by output buffer as shown in fig 1. Since all internal nodes of OTA are low impedance node except input and output nodes, buffer is used as isolation between load and OTA. OTA only drives small capacitive load while the load to practical op-amp can be resistive or capacitive or combination of both. Since the load is connected at the output of the op-amp, which is a low impedance node, the load capacitance has little effect on the phase margin of the amplifier. Therefore, the OTA should be internally compensated; in order that the overall amplifier would exhibit poor stability.

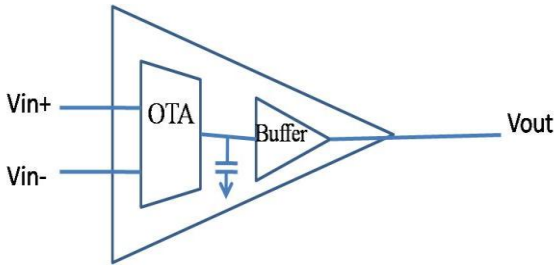



*Fig. 1 Conventional Op-amp*

As shown in fig 1, in conventional op-amp, the OTA is compensated using capacitor which connects output of OTA to ground. The high speed Op-amp method presented in this paper is illustrated in Figure 2. In addition to conventional circuit structure, the OTA is additionally compensated using a Miller capacitance connected between the input and output of the buffer.

Assuming that the Op-Amp drives a parallel combination of a capacitor CL and a resistor RL, the effective capacitance seen at the input and output of the buffer is

$$C_{effin} = C_c(1 - A) + C_{c(conventional)}$$

$$C_{effout} = C_L + C_c\left(\frac{A-1}{(A)}\right)$$

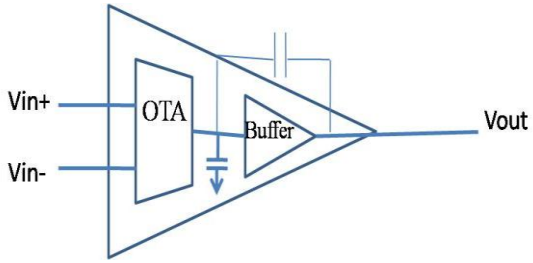



*Fig. 2 Proposed compensation in addition to conventional*

Since the gain of the buffer is always smaller than one, the effective capacitance seen at the output of the Op-Amp is smaller than the original load capacitance. This effect pushes the first non-dominant pole (*i.e.*, the pole closest to the origin after the dominant pole) to a higher frequency. The location of the dominant pole, however, remains unaltered. This argument suggests that in the proposed compensation scheme, both the unity gain frequency and phase margin are improved as compared to a conventional circuit structure.

Miller capacitance compensation is extensively used in two-stage Op-Amps and other applications [4]-[7]. Generally speaking, in these applications, the Miller capacitance is connected around an amplifier with a negative high gain

The reason for this negative gain is to establish negative feedback. In the approach presented here, the gain of the buffer is positive (but smaller than one). As long as the gain is smaller than one, the positive feedback does not necessarily result in a completely unstable system, as shown in this paper.

This paper presents the application of a negative Miller capacitance to reduce the effective load capacitance so as to achieve both a higher bandwidth and improved phase margin.

## 3. DESIGN AND IMPLEMENTATION

In this section, the op-amp is designed and the above compensation technique is incorporated in it. The proposed op-amp consists of single ended OTA connected with output stage of push-pull buffer. The amplifier is designed based on a 65nm standard CMOS process from IBM and achieves 86.719 dB DC gain. The unity gain frequency and phase margin of the amplifier are 34 MHz and 84°, respectively, for 5 pF load. The power consumed by the Op-Amp is 0.3 uW with a 1.5 volt single power supply.

The schematic of the above design is shown in fig 3. The OTA core is made up of single ended folded cascode topology. The folded-cascode topology provides limited gain (usually, between 60 dB and 65 dB) in deep sub-micron CMOS technologies due to the low intrinsic impedances of the devices.

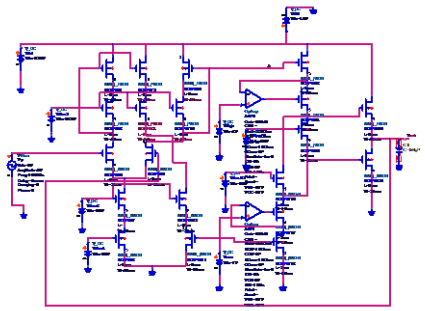
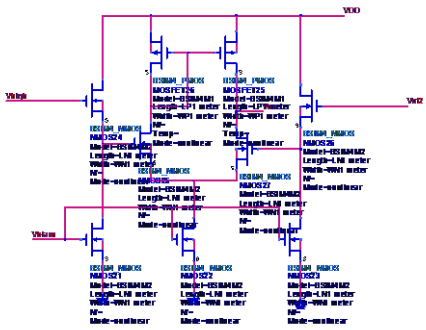


*Fig 3. Schematic of proposed op-amp*

In this paper, the DC gain of the OTA is increased by Gain Enhancement Technique. For this, auxiliary gain boosting amplifiers with a single-ended folded cascode topology is used (fig. 4). All of the voltages required for biasing the OTA core (fig 3), auxiliary amplifiers (fig 4) and buffers (fig 5) are generated using a self-biasing circuit (fig 6). The remaining components of the Op-Amp are explained in greater detail in the following paragraphs.

As mentioned previously, the gain enhancement amplifiers are implemented using single-ended folded-cascode gain stages as shown in Figure 4. Compared to a common source amplifier, folded-cascode gain stage provides higher lower frequency gain. However, the cost for this enhancement is a small increase in power consumption and area. Two amplifiers are designed i.e N-amplifier and P-amplifier. These are used here to compensate for the low gain caused by minimum channel length in sub-micron region. These are configured as source follower which allows the amplification of signal near ground for P-Amplifier or near VDD for N-amplifier. It works as level shifter in this proposed op-amp circuit.



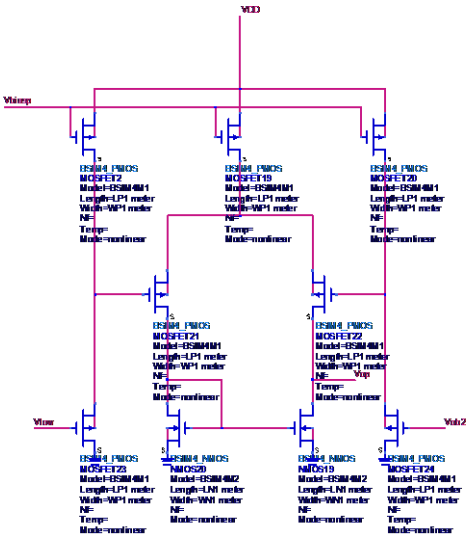


*Fig. 4 Diff amps with source follower level shifter to be used in Gain Enhancement*

The low frequency open loop gain of the op-amp depends on the load resistance. If output buffer is not used the gain of op-amp is significantly affected by load value. The output of second stage is isolated from the load by adding buffer stage. Fig 5, shows the output buffer stage. The compensation capacitor is added in between input and output of output stage to push the pole deeper and increase low frequency gain.

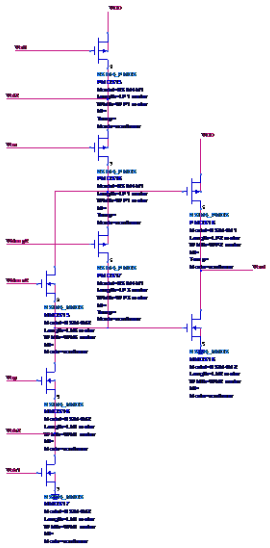


*Fig. 5 Class AB push pull Output buffer stage*

A schematic of the threshold voltage referenced self-biasing circuit is illustrated in Figure 6. The circuit is used to generate the voltages required to bias the OTA core, auxiliary amplifiers and buffers. Note that a start-up circuit (PMOS1, NMOS1 and NMOS2) is utilized to avoid zero current flow in the current generator. The subsequent circuits are used to generate the remaining biasing voltage required (fig. 6(b) – fig. 6(c)).

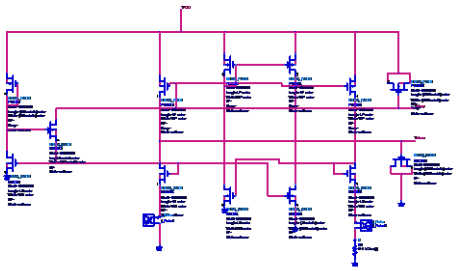


*Fig. 6(a) Self bias circuit to generate bias voltage*

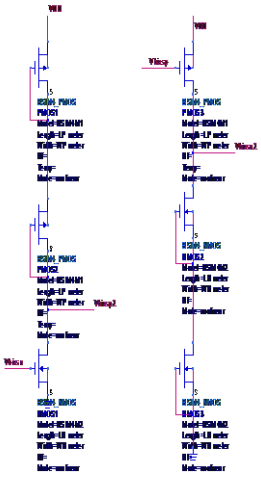


*Fig. 6(b) Biasing voltage for auxiliary amplifier*

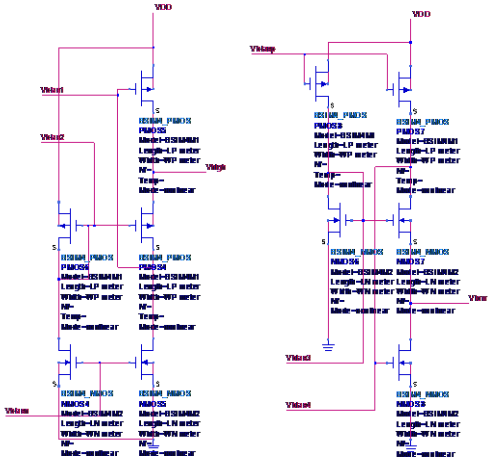


*Fig. 6(c) Biasing voltage for output buffer stage*

## 4. SIMULATION AND ANALYSIS

Agilent's Advanced Design System version 2009 is used for performing the simulations. With the following operating condition, the circuit is simulated.

Operating temp. --- Room temperature
Power Supply voltage --- 1.5V
Input bias current --- 200nA

Fig. 7 shows DC transfer curve showing relation between input DC voltage and output DC voltage in open loop configuration. The offset voltage is about 0.03 V which is very large. DC gain is 86.719 dB which is desirable.

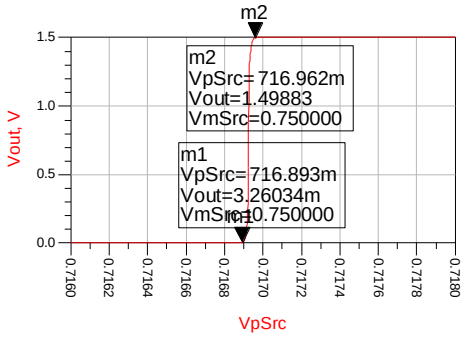



*Fig. 7 DC transfer curve*

Fig. 8 shows gain and phase plot of op-amp with input at non-inverting point. The unity gain frequency is 34MHz and the obtained phase margin is 84$^o$ which is good for low power low voltage op-amp.

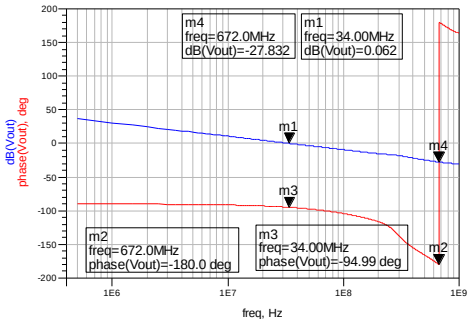



*Fig. 8 Gain and Phase plot*

Fig. 9 shows the transient behaviour of the designed op-amp. This circuit is configured as inverting amplifier with 22pF pure capacitive load.
The waveform shows excellent settling time and slew rate.

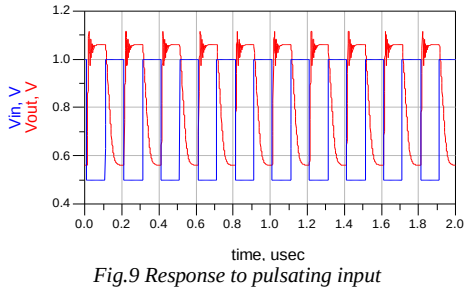



*Fig.9 Response to pulsating input*

To obtain the values for settling time and slew rate, the same circuit as of Transient Analysis is excited by step input voltage having input level of 0.5V to 1.0V. The settling time (2% of final value) comes out to be 50ns which is very much acceptable. The slew rate is calculated by obtaining maximum rate of change of output voltage. The slew rate of this designed op-amp is 72.7V/µs. It is very good for technology in consideration.

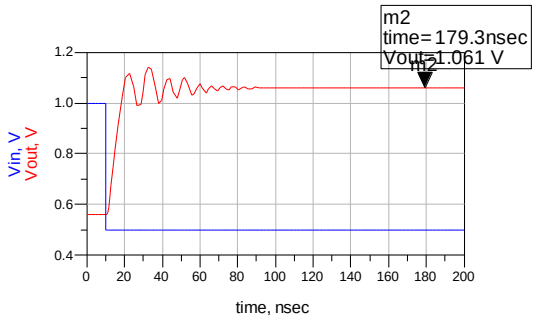



*Fig. 10 Response to step input*

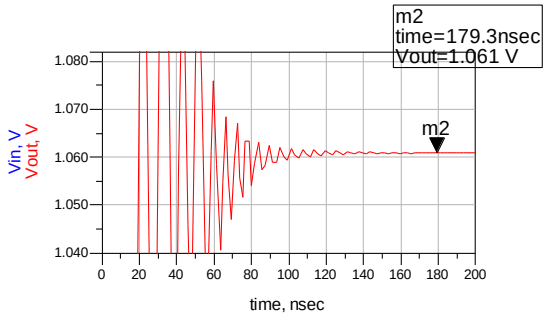



*Fig. 11 2% window of final value*

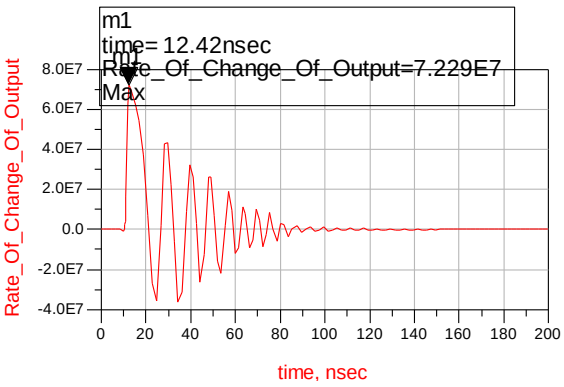



*Fig. 12 Rate of change of Output Voltage to calculate slew rate*

## 5. CONCLUSION

The method presented is efficient in compensating the buffered op-amp. In this, OP-Amp is compensated by capacitor connected between input and output of output buffer. The results obtained shows 86dB gain, 34MHz unity gain frequency, 83$^o$ phase margin which are in line with available reported op-amp of same process technology. It also has high slew rate and less settling time to make the circuit work faster. The only drawback is increased offset voltage. Although input offset voltage is not at acceptable level, the other results are acceptable to present industry standard.

## 6. REFERENCES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