A Novel Architecture for Current-steering Digital to Analog Converters

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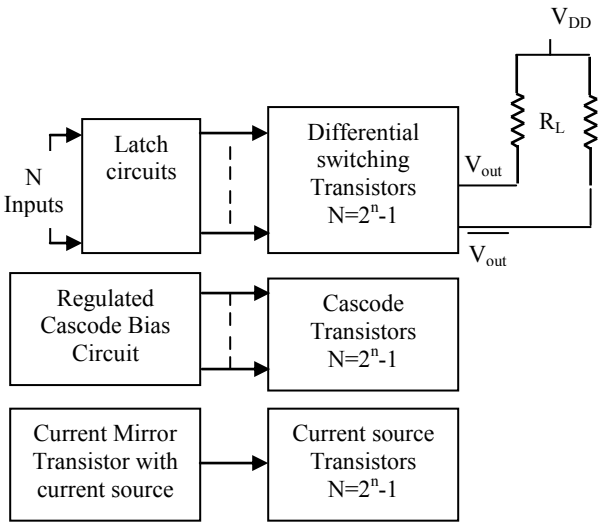
***Abstract* — This paper presents a novel Current Steering Digital to Analog Converter architecture to reduce area as well as power dissipation. The current cells of conventional binary weighted architecture require larger size of transistors for MSBs. In this paper, same sized current cell transistors for MSBs as that of LSBs and a current mirror circuit is used between the load and MSBs to provide necessary higher current. Here, 6-bit CS-DAC is simulated. The area of this proposed CS-DAC has decreased by about 12% and power dissipation by about 50% in comparison with a conventional Binary architecture.**

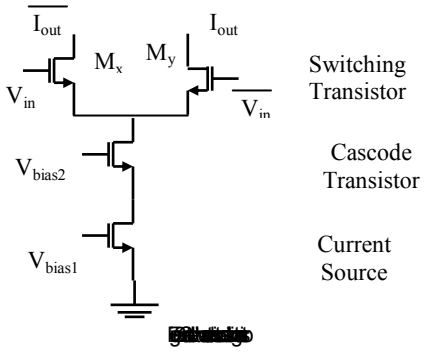
***Keywords*—data converters, digital-to-analog, current steering, current mirroring,cascode**

I. Introduction

Digital to analog converters required by digital signal processors, medical instruments, wireless communication and other various processing equipment has proved to be a continuous challenge for the analog designers to improve and develop new DAC architectures. Current steering DAC is most popular due to its high speed, high resolution and small size [1,2,3]. The basic block diagram of Current Steering DAC(CS-DAC) is shown in Fig.1.



It has (2^n-1)current source transistors with cascode circuits and switching transistors. Static and dynamic performances of current-steering DACs are mostly determined by the accuracy of the current sources, Non-infinite output impedance and switching time. The current cells with cascaded topologies as shown in Fig.2, are satisfactory for static and dynamic output impedance requirements [2] [3].



In this paper, design of a 6-bit Current Steering DAC has been reported. The technology used for the design is 180nm CMOS process. Larger sizes of current cell transistors at MSBs are avoided in this architecture by using Current mirror circuit.

The paper is organized as follows. A review of the conventional architecture in given section II, the proposed architecture and its design considerations is described in section III. Simulation results are given in section IV followed by the conclusions in section V

II. DAC architecture

A. *The Binary Architecture*

In this architecture, each digital input directly controls the binary weighted unit current sources that are switched to the output in a successive manner. N bit binary weighted CS-DAC architecture is shown in Fig.3.

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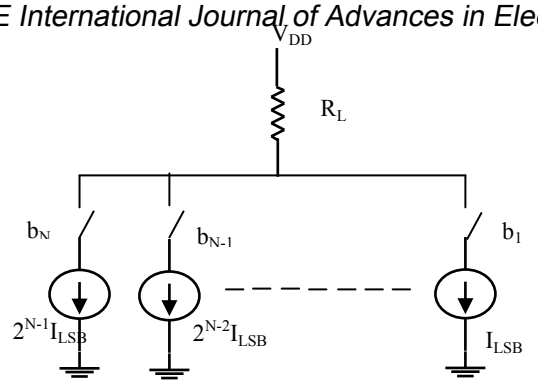


Figure 3 N-bit Binary Weighted CS-DAC

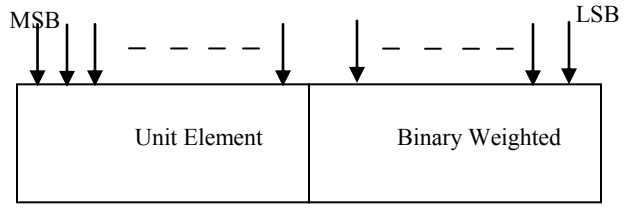
This architecture is implemented on a small silicon area and it minimizes the digital power consumption. However, the most significant bits (MSB) in this architecture control large currents that are affected by mismatch errors. A large DNL error may occur when switching on the MSB and all the other bits off, which leads to a severe degradation of the static performance for this architecture [2].

B. *The Unary Architecture*

In the unary architecture, the current source array consists of $(2^N - 1)$ unity current sources that can be accessed separately. The digital input code has to be converted to a decimal code that determines the number of current sources to be switched to the output. Binary to unary decoder is required for this architecture. This decoder consumes a lot of silicon area and has large power consumption, thereby offering a good DNL specification. Only one extra unity current source needs to be switched to the output when the digital input value is increased by one [2].

C. *The Segmented Architecture*

In order to obtain architecture with a good DNL specification having an acceptable power and a minimum area, a combination of the previous two architectures, known as Segmented architecture, is chosen. This architecture is widely used in high-speed and high-accuracy digital-to-analog converters (DAC's) [1], [4]–[7]. Fig.4 shows a segmented current steering DAC (CS DAC) architecture, in which the least significant bits (LSB's) are realized using a binary-weighted array and the most significant bits (MSB's) are implemented with an unary array(thermometer decoded) .



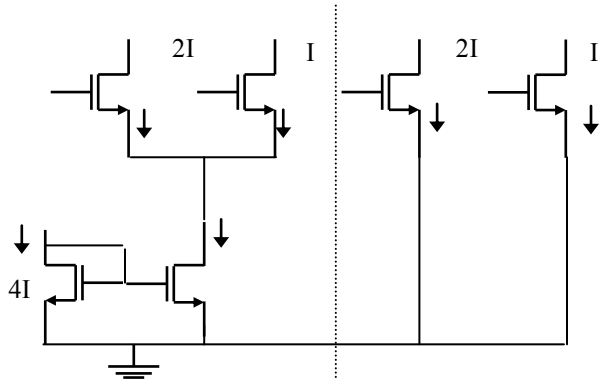
Increasing the number of thermometry bits guarantees the monotonicity, reduces the glitch energy (caused by timing mismatch error of the switches while the input code is changing), reduces the total harmonic distortion and increases the linearity of the converter [1].

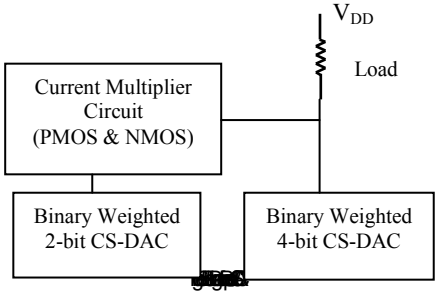
III. Proposed Architecture

For higher resolution, Binary weighted CS-DAC require larger size of current source and segmented CS-DAC architecture consumes more die area [4,5]. In order to compensate this recede, a new architecture is proposed. In this design, current mirror circuit for MSBs is used instead of Unit Elements, as shown in Fig. 5.

The proposed DAC is based on the current mirror circuit concept, where the width of MSBs current source transistors is kept same as the width of LSBs. The Block diagram of proposed CS-DAC is as shown in Fig. 6.

Here, two current mirror circuits are employed between the load and current source transistor. PMOS current mirror circuit is used as a multiplier for higher MSBs instead of NMOS, as the amount of current mismatch error is more in NMOS[2] because of the higher mobility of electrons. Cascode transistor with mirror transistor helps to improve linearity of DAC[6]. Use of regulated cascode bias circuit is as shown in Fig. 7. Regulated cascade circuit has an added advantage of providing high impedance and high swing compared to other cascode circuits [8]. Due to the feedback mechanism, output voltage variation keeps current source transistor (T1) in saturation. Desired load current and equivalent analog output voltage across the load is achieved with this proposed architecture.





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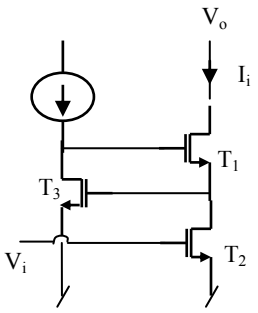


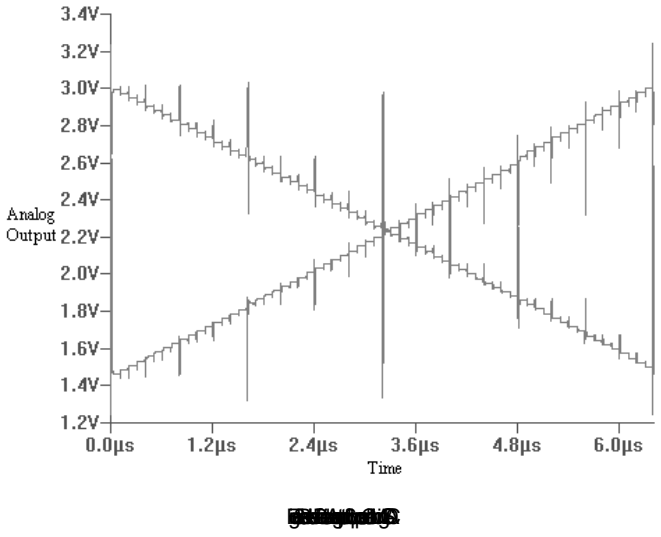
Figure 7 Regulated Cascode Circuit

IV. Simulation Results & Discussion

. The 6-bit current steering DAC is simulated on LTSpice using 180nm technology. The power consumption of the proposed DAC is about 0.87mW at 3V power supply. The core size of the proposed DAC is about 0.26mm^2. Thus the area of the proposed DAC is smaller by 12% than that of conventional DAC and power dissipation is reducing by 50%.

The Proposed CS-DAC has a monotonic behavior. There is an initial rising time due to current mirror circuit present across the load. To avoid this, extra switches are used between current mirror circuit and load. Fig. 8 shows DAC output with glitch energy of 14nS.V Extra switches are responsible for this larger glitch energy.

The 6-bit Current Mirroring CS-DAC Real as well as differential output is shown in Fig. 8.



The measured DNL and INL errors are less than 0.15 LSB as shown in Fig. 10.

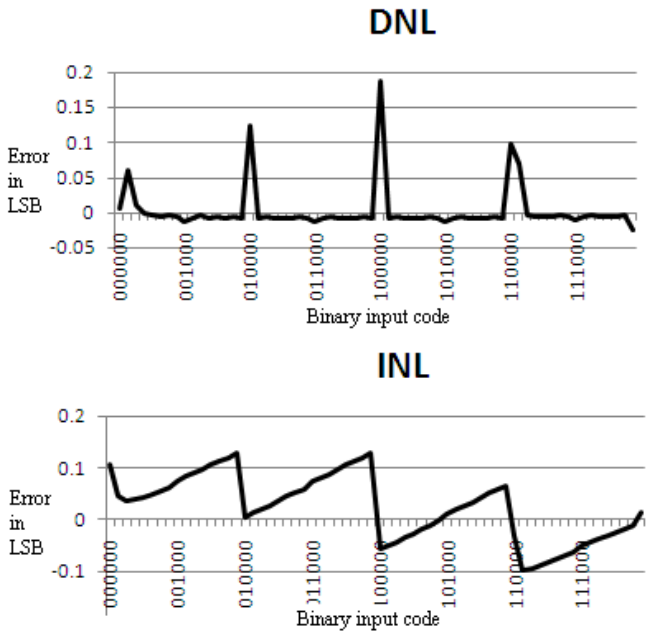
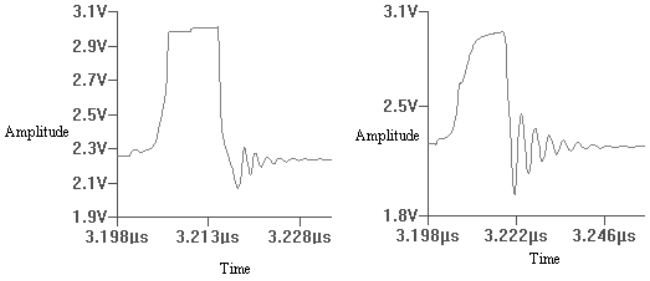


Figure 9 DNL and INL of 6-bit Proposed Current Mirroring CS-DAC

The maximum glitch energy is observed at transition from 011111->100000. Fig. 11 shows comparison of this glitch with binary weighted CS-DAC, which is 20% higher compared to binary weighted CS-DAC.



V. Conclusion

From this work, it can be concluded that the incorporation of current mirror circuit in the design of analog circuits helps to avoid larger width of current source transistors at MSBs to get higher current. Further, the area and power dissipation of the proposed DAC architecture is less as compare to the other DAC architectures. The performance of the circuit is summarized in Table. 1.

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TABLE I. PERFORMANCE COMPARISON

Performance Parameter	***Binary Weighted CS-DAC***	***Proposed Design***
Resolution	6-bit	6-bit
Technology	180nm	180nm
DNL	0.13LSB	0.13LSB
INL	0.13LSB	0.13LSB
Glitch Energy	12nsV	14nsV
Power Supply	3v	3V
Power Dissipation	1.9mW	0.87mW
Chip Area (DAC Core)	0.292mm^2	0.262mm^2

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