High Performance Latch Design for Portable Application

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***Abstract*— In recent years, low power design has become one of the main focuses of digital VLSI circuits. As technology scales, leakage currents in contemporary CMOS logic have become one of the main power consumers. Contrary to conventional methods for power reduction, where efforts are taken to reduce sub-threshold leakage, operation of digital circuits in the sub-threshold region utilizes this current to minimize power consumption in low-frequency systems. This research paper proposes novel design of 8-transistor latch. The design performance is evaluated by comparing it with the conventional design of the latch. The simulation results are analyzed at 65nm and 45nm technology to show the technology independence of the design. The proposed design of latch is better suitable for the low power VLSI applications.**

Keywords- Level converting Flip Flop, Portable Applications, Latch, Sub-threshold Region, Low Power applications.

I. INTRODUCTION

Low power device design is now a vital field of ever research due to increasing in demand of portable devices [1]. Digital integrated circuits commonly use CMOS circuits as building blocks. The trend of decreasing in feature size of CMOS circuits and corresponding increase in chip density and operating frequency is the compelling concern of power consumption in VLSI design. Excessive power dissipation in integrated circuits, not only discourages their use in portable environment but also causes overheating, reduces chip life and degrades performance. Minimizing power dissipation is therefore important, both for increasing levels of integration and to improve reliability, feasibility and cost. Power dissipation can be reduced by scaling the supply voltage. The scaling of supply voltage linearly with feature size was started from half-micron technology. But the power supply scaling affects the speed of the circuit .The need of the time is to put efforts in designing low-power and high speed circuits.

Flips-flops and latches are some of the most frequently used elements in digital VLSI systems. In synchronous systems, flip-flops are the starting and ending points of signal delay paths, which decide the maximum speed of the systems. Since, they are clocked at the system operating frequency; flip flops consume a large amount of power [2]. About 30%-70% of the total power in the system is dissipated in clocking network and the flip-flops [3].

Flip-flops and latches are indispensable components of every sequential system. A large portion of the clock power is used to drive these sequential elements. Reducing the clock power dissipation of flip-flops and latches is of prime concern for the total chip power reduction [4].

If the battery life is the only concern, then the energy (that is, the power-delay product) should be minimized. In this case the battery consumption is minimized even though an operation may take a very long time. On the other hand, if both the battery life and the circuit delay are important, then the energy-delay product must be minimized. In this case one can alternatively minimize the energy/delay ratio (that is, the power) subject to a delay constraint. In most design scenarios, the circuit delay is set based on system-level considerations, and hence during circuit optimization, one minimizes power under user-specified timing constraints.

Latch is the fundamental component for the processor storage. Latches and Flip-Flops are the most complex, power consuming and indispensible components among the various building blocks in digital designs. Latch is the basic sequential elements for the purpose of synchronizing data signals. A latch is a three-terminal element, having two inputs, data (D) and clock (clk) and one output (Q). Flip flop and Latch commonly used sequential elements for synchronizing data signals. The data must be stable before the falling edge of the clock and after the falling edge of the clock for correct storage in the latch. The level sensitive latches are widely used in high performance ICs where timing analysis is more critical and challenging [5-7]. The conventional edge-triggered flip-flop (FF) design methods using clock synchronization are very practical, since only the timing constraints defined by a given clock frequency are optimized. However, clock skew that has a strong influence on clock frequency design prevents the FF design because of the variations. Thus, level-triggered latch design method has been proposed as alternatives to FF-based design methods.

For $V_{GS} < V_t$, there are less minority carriers in the channel, but their presence comprises a current and the state is known as weak-inversion. In standard CMOS design, this current is a sub-threshold parasitic leakage, but if the supply voltage (V_{DD}) is lowered below V_t, the circuit can be operated

using the sub-threshold current with ultra-low power consumption Sub-threshold circuit operation is driven by currents much weaker than standard strong-inversion circuits, and this is characterized by longer propagation delays and limited to lower frequencies. Due to the exponential dependency on the value of V_t, sub-threshold circuits are very sensitive to process variations and temperature fluctuation. These along with other factors, have to be taken into consideration when designing circuits for sub-threshold operation.

The total energy dissipation E_T of static CMOS circuits operating in sub-V_T regime is modeled as

$$E_T = E_{dyn} + E_{leak} + E_{sc}$$

$$E_T = \alpha C_{tot} V_{DD}^2 + I_{leak} V_{DD} T_{clk} + I_{peak} t_{sc} V_{DD}$$

Where, E_{dyn}, E_{leak}, and E_{sc} are the average energy dissipation due to switching activity, the energy dissipation resulting from integrating the leakage power over one clock cycle T_{clk}, and the energy dissipation due to short circuit currents, respectively. The energy dissipation E_{sc} has been shown to be negligible in the sub-V_t regime [8]. The dynamic power dissipation, since the input and voltage and the supply voltage are less than the threshold voltage of the transistor, is also very less as compared with the super-threshold operation of the device. The dynamic and leakage power dissipation is only results from sub-threshold currents [9].

The critical path delay in CMOS devices is related to the clk as [10]

$$T_{clk} = k_{crit} \frac{C_{inv} V_{DD}}{I_o e^{\frac{V_{DD}}{nV_T}}}$$

Where, k_{crit} is the critical path delay, n denote the slope factor and and V_T the thermal voltage. The total energy dissipation E_T assuming operation at the maximum frequency is

$$E_T = C_{inv} V_{DD}^2 [\mu_e k_{cap} + k_{crit} k_{leak} e^{-\frac{V_{DD}}{nV_T}}]$$

It is found that the sub-V_T model predicts the energy dissipation with less than 3.8% error [11].

There are three main sources of power dissipation in the latch [12]:

- *Internal power dissipation* of including the power dissipated for switching the output loads.
- *Local clock power dissipation*, presents the portion of power dissipation in local clock buffer driving the clock input of the latch
- *Local data power dissipation*, presents the portion of power dissipation in the logic stage driving the data input.

Total power parameter is the sum of all three measured kinds of power.

In this paper, an elegant design of latch with 8-transistor is proposed. The design is compared with the conventional design of 8-transistor latch for power dissipation, delay and area as parameters. The proposed and the conventional designs are simulated and analyzed at 65nm and 45nm technologies to show the technology independence.

The rest of the paper is organized as follows. In Sect. 2, we describe the proposed latch structure and its behavior along with the conventional latch. In Sect. 3, we report simulation analysis and some comparison results. Conclusions results are drawn in Sect. 4 and finally Sect. 5 contains references.

II. Latch Design

A. Conventional 8T design

The conventional 8 transistor latch design uses transmission gate logic [13]. The output Q assumes the value of the input D when the clock is active, i.e. for CLK=1. When the clock signal goes to zero, the output will simply preserve its state. Thus the clock input acts as an enable signal which allows data to be accepted into the D-latch.

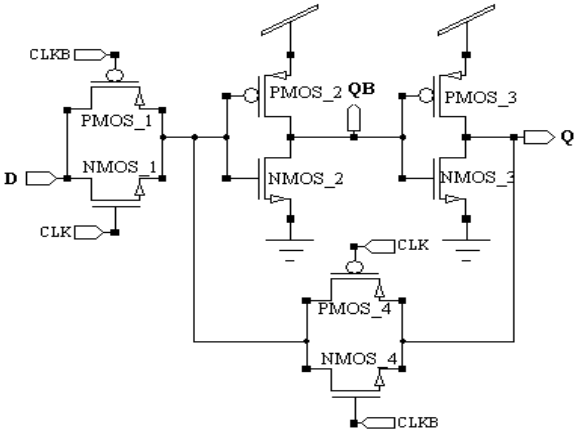

Figure. 1 Conventional 8 Transistor Latch

This circuit basically contains two inverter loop and two transmission gate (TG) switches. The TG at the feedback loop is activated by the inverse of CLK signal, CLKB. Thus the input is accepted (latched) into the circuit when the CLK is high, and the information is preserved as the state of the inverter loop when the CLK is low. The conventional latch is positive level triggered.

B. Proposed 8T design

The proposed 8-transistor design implements pass transistor logic for the transmission of data through it. The drain of first nMOS transistor and pMOS_1 are connected to the data input and this data will be available at the drain terminal only when the clock will be low.

Since the pMOS transistor are weak zero transistor, so the small threshold loss is observed when data is zero. But overall performance of the device is almost unaffected because of the presence of the inverters.

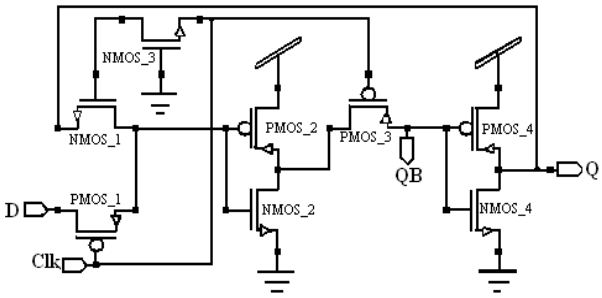

Figure. 2 Proposed 8T Latch Design

The nMOS_3 transistor at the path works as a delay element on a charge sharing basis. The transistor nMOS_1 passes the output according to the delayed version of the clock. Thus whenever clock is high, data is not passing through the transistor pMOS_1 but output is again feedback through the circuit and output remains same. Thus this proposed clocked latch acts as a negative level triggered flip flop. Whenever, clock is negative, the output changes with respect to data but remains constant as clock goes positive (Figure. 3). The output remains unaffected even if clock is absent, thus the proposed latch is static in nature.

For the purpose of delay element, nMOS is preferred over pMOS because nMOS has less resistance and hence shows less power consumption, and also NMOS is faster than pMOS.

III. SIMULATION AND ANALYSIS

The conventional and the proposed designs are simulated using Tanner Tools v13.0 and power consumption and delay produced are measured at various temperatures, supply voltages and frequencies.

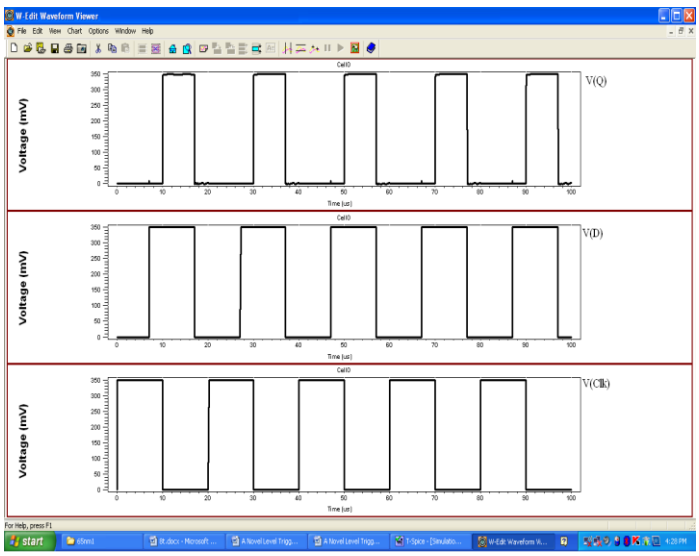

Figure 3. Input Output waveform of prposed 8t latch

The designs are compared at two different technologies BSIM3v3 45nm and 65nm with varying temperature, supply voltage, frequencies keeping APC, Delay and PDP as parameters. In low power applications area, power consumption, and delay introduced by the device are the main technological aspects to prefer a design over the other conventional latch. The standard values of temperature, voltage and frequency are taken to be 25°C, 0.35V and 1 MHz respectively. During simulation one value is varied keeping other two constant.

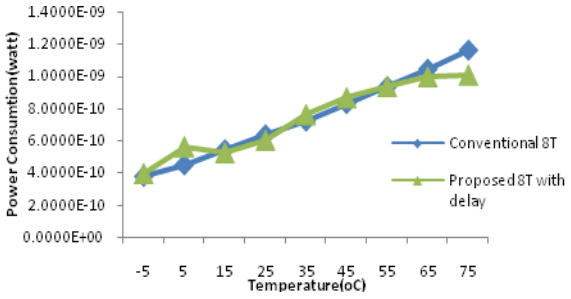

Figure. 4 Average power consumption at various temperatures (°C) in 65nm technology

As temperature increase, than because of increase in thermal generation and recombination rate, the characteristics of the semiconductor device are affected. Thus, average power consumption and delay of the device are affected with temperature as the collision rate of the carriers increases and some of the power is consumed in the form of thermal energy. From the above graph (Figure.4) it is clear that the power consumption of both the designs are almost comparable, but delay introduced by the proposed design is remarkably low, so PDP is preferable.

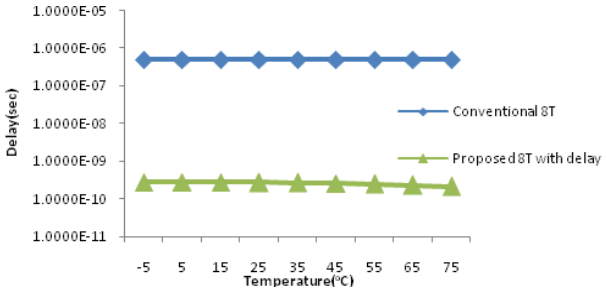

Figure. 5 Delay at various temperatures (°C) in 65nm technology

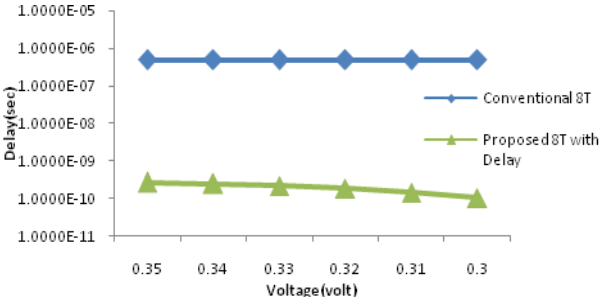

Figure. 6 Delay at various supply voltages (V) in 65nm technology

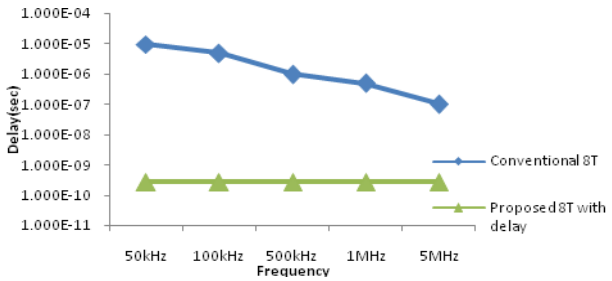

Figure. 7 Delay at various frequencies in 65nm technology

All delay graph (Figure.5 – Figue.10) are logarithmic curves. From Figure.5 – Figure.7 it can be seen that delay introduced by proposed design is hundred to thousand times lower than the proposed design.

Same results are obtained when simulation is done at 45nm technology. The average power consumption by the proposed latch at various temperatures, supply voltages and frequencies is almost comparable to the conventional latch in 45nm technology. Similarly the delay introduced in proposed design is reported much less than the contending design (Figure.8- Figure.10).

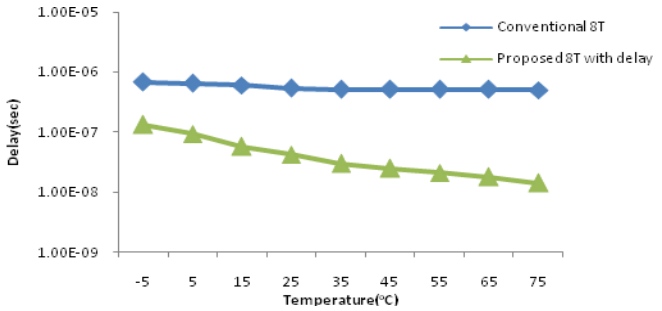

Figure. 8 Delay at different temperatures (°C) in 45nm technology

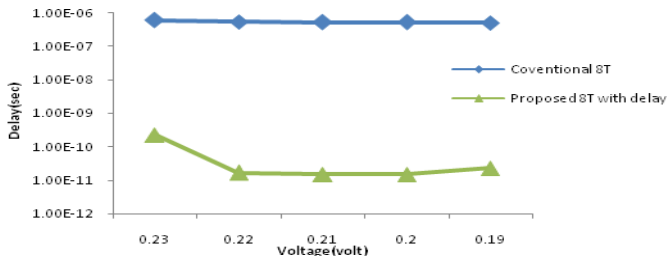

Figure. 9 Delay at various supply voltages in 45nm technology

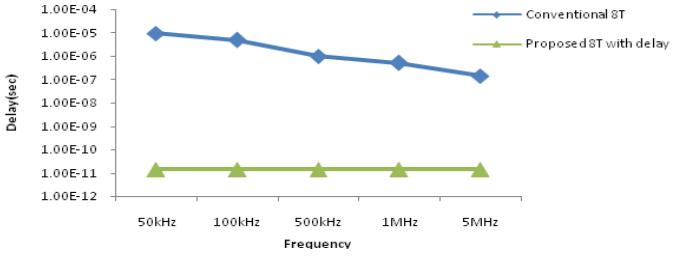

Figure. 10 Average Power Consumption at various frequencies in 45nm technology

For low power applications, the devices work up to medium frequencies. The two designs are compared up to 5MHz frequency and reveals that the proposed design introduces less delay (Figure. 9).

From the above mentioned comparisons, it is clear that one of the parameters in VLSI design, i.e., power delay product of the proposed design is always better than the conventional design irrespective of technology or parameters (e.g., temperature, supply voltage and frequency) incorporated.

IV. CONCLUSION

The proposed design have almost comparable power dissipation and significantly reduced delay resulting in much less power delay product of the order of thousands of times lesser than conventional one. The proposed clocked latch design shows better performance in two different technologies, so the design passes technology independence parameter. Thus the proposed design is very much useful for low power application and it will certainly provide better performance than old one.

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