Low Power 1-Bit 9T Full Adder Cell using XNOR Logic

Shiwani Singh, Tripti Sharma, K. G. Sharma and Prof. B. P. Singh
Electronics and Communication Department
FET- MITS (Deemed University)
Lakshmangarh, Distt. - Sikar, India
e-mail: mits.shiwani@gmail.com, tripsha@gmail.com, sharma.kg@gmail.com, bpsinghgkp@gmail.com

***Abstract*— In this paper a new low power and high performance 9T adder circuit using XNOR gate architecture is proposed which improves the performance of existing 8T adder by sacrificing the MOS transistor count by one. Simulation results demonstrate the superiority of the proposed adder against existing 8T adder in terms of power consumption and temperature sustainability. The combination of low power and better temperature sustainability makes the proposed full adder an optimal option for low power and energy efficient design. All simulations are performed on 90nm standard model on Tanner EDA tool version 13.0.**

***Keywords*—8T, 9T, XNOR gate, full adder and low power.**

I. INTRODUCTION

The increasing prominence of portable systems and need to limit power consumption has led to rapid and innovative developments in low power VLSI design during recent years. The driving forces behind these developments are portable device applications requiring low power consumption and high throughput.

The need for low-power design is also becoming a major issue in high performance digital systems, such as microprocessor, digital signal processors (DSPs) and other applications. Adder is one of the most important building block of a processor [1] and [2]. So, obviously, enhancing the performance of adder cell will improve overall system performance.

In this paper, the power results of the proposed 9T adder have been compared with the existing 8T adder with varying input voltages, supply voltages, frequencies and temperatures. As a result the proposed design is found to be efficient with negligible area overhead.

This paper is organized as follows: Section II describes the existing 8T full adder cell reported in the literature. Section III describes the design and functionality of proposed 9T full adder. Simulation results and their comparisons are presented in Section IV and finally Section V draws the conclusion.

II. PRIOR WORK

The full adder operation equations given below can be stated as follows: Given the three 1-bit inputs A, B and Cin, the Sum and Carry outputs can be calculated as

$$\text{Sum} = (A \text{ xor } B) \text{ xor } Cin \quad (1)$$

$$\text{Cout} = A \text{ and } B + Cin\ (A \text{ xor } B) \quad (2)$$

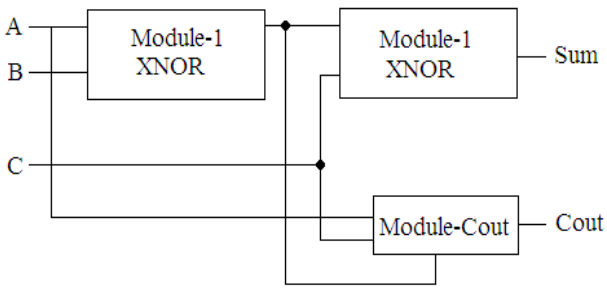

Figure 1. Basic Architecture of 8T Full Adder

The basic architecture of the 8-T full adder [3] and [6] which consists of 3 modules is shown in Fig. 1. The sum and carry are obtained using (1) and (2) respectively. The module-1 and module-2 are taken as XNOR gates and hence, the Sum output is obtained by a cascaded EX-NORing [3]-[5] of the three inputs and Cout is implemented using 2T multiplexer [3] and [5].

The schematic of eight transistor 1-bit full adder cell is shown in Fig. 2. The voltage drop due to threshold loss in

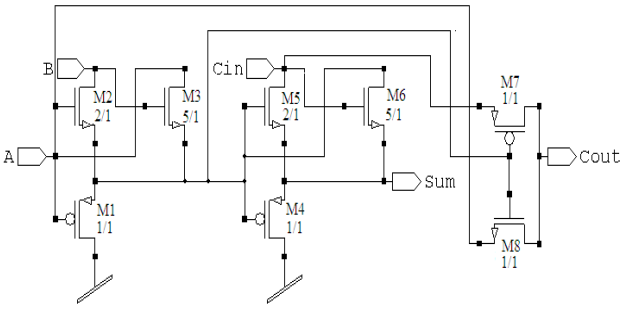

Figure 2. 1- Bit 8T Full Adder

transistors M3 and M6 can be minimized by suitably increasing the aspect ratio of these two transistors. Although, this circuit operates efficiently in super threshold region but due to degraded Sum output it consumes very high power which increases drastically with increasing input voltage and supply voltage and temperature sustainability is very large which is not suitable for low power applications.

III. PROPOSSED 9T FULL ADDER DESIGN

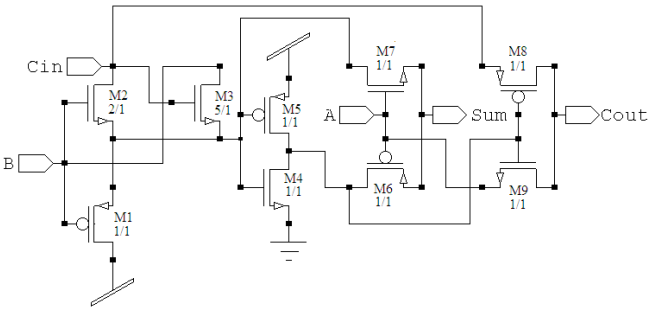

Figure 3. Proposed 9T Full Adder

The schematic of proposed 9T full adder cell is shown in Fig. 3 and its truth table is stated in Table I. The operating principle of proposed circuit is different from conventional logic. The operation of full adder in its conventional form can be calculated as given in (1) and (2).

For generating the Sum output in the proposed design, the truth table has been divided into two parts, one for input A='0' and another for A= '1' rather than implementing the conventional Sum module. From the truth table shown in Table I it is evident that when A= '0', Sum can be produced by XORing inputs B and Cin. Similarly, when A= '1', Sum is showing the XNORing between inputs B and Cin. Therefore, the operation of Sum module is based on implementing XOR operation and XNOR operation between inputs B and Cin. An inverter is connected at the output of first stage XNOR gate to generate XOR function. Finally the Sum is implemented by transferring these output levels through 2T multiplexer. Input to PMOS transistor M6 is XOR of B and Cin while to NMOS M7, input is XNOR of B and Cin. This 2T multiplexer is controlled by input A. Cout is implemented by using another 2T multiplexer which is controlled by output of first stage XNOR gate and passes either A or Cin accordingly. This circuit efficiently operates in super threshold region thereby improving power consumption and temperature sustainability remarkably.

TABLE I. TRUTH TABLE OF 1-BIT FULL ADDER

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The proposed circuit has area overhead of one transistor but still its power consumption is reduced and remains constant with increasing input and supply voltages than its peer design. The 8T adder circuit in Fig.2 has 2/1 aspect ratio of M5 and 5/1 aspect ratio of transistor M6 in order to drive Sum output to logic high but the adder shown in Fig. 3 has 1/1 aspect ratio of all the transistors (M4-M7) connected in second stage of Sum module. Therefore, the proposed design will not affect the area by large extent. In a nutshell, the proposed 9T full adder has better performance than existing 8T full adder.

All the substrate terminals in Fig. 2 and Fig. 3 are connected to their respective source terminals in order to nullify the substrate-bias effect.

IV. SIMULATION AND COMPARISON

All schematic simulations are performed on Tanner EDA tool version 13.0 at 90nm technology with input and supply voltage ranging from 1.0 V to 2.0 V in steps of 0.2 V. The proposed full adder is analyzed in terms of power at varying input voltages and supply voltages, frequencies and temperatures. To establish an impartial testing environment both circuits were simulated on same input patterns which covers each and every combination of the input stream.

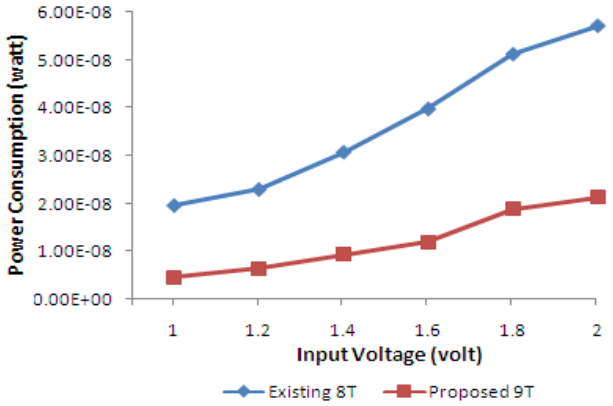

Figure 4. Power Consumption with increasing input voltage and supply voltage

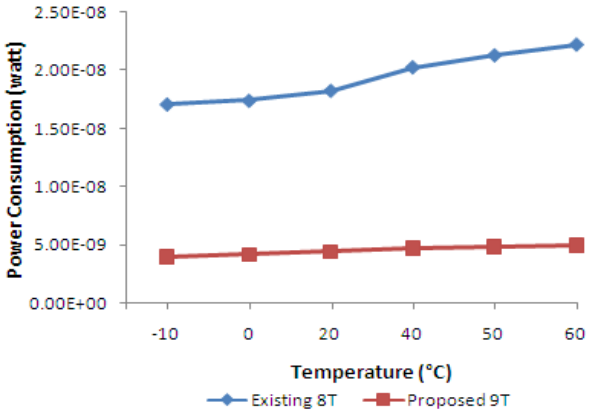

Figure 5. Power Consumption with varying temperature at 1V Input voltage and Supply voltage

Fig. 4 depicts that the proposed 9T adder has reduced power consumption with increasing input and supply voltages when compared with 8T full adder circuit.

Comparison in terms of power consumption with increasing temperature is shown in Fig. 5 and the result reveals that the proposed 9T full adder cell has better temperature sustainability which remains constant over large range of temperature than existing 8T adder. Similarly Fig. 7 shows the comparison of power consumption with increasing

operating frequency and still the proposed adder cell has better results than the existing one.

Therefore, it is clearly evident from the above simulation results that proposed 9T adder can undoubtedly be a better choice for low power system design.

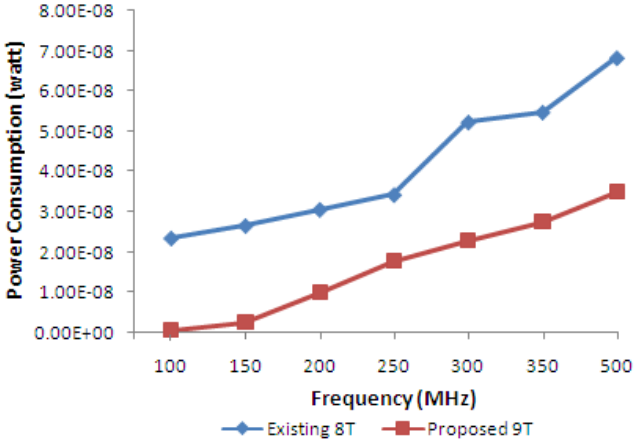

Figure 6. Power Consumption with increasing operating frequency

V. CONCLUSION

The simulation results demonstrate that the proposed 9T adder when compared with the existing 8T adder proves to be an easier solution for significant improvement in power consumption as well as temperature sustainability while achieving higher performance at the cost of negligible area overhead. The proposed 9T adder has been designed and studied using 90nm technology and proved itself to be a better option for ultra low power complex system design.

REFERENCES

[1] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design, A System Perspective*. Reading, MA: Addison-Wesley, 1993.

[2] S. Kang and Y. Leblebici CMOS Digital IntegratedCircuits, Analysis and Design, 3rd ed.

[3] S.R.Chowdhury, A. Banerjee, A. Roy, H. Saha, " A high speed 8 transistor full adder design using novel 3 transistor XOR gates," *International Journal of Electronics, Circuits and Systems*, Vol. 2, No. 4, Fall 2008, pp. 217-223

[4] Sreehari Veeramachaneni, M.B. Srinivas, "New Improved 1-Bit Full Adder Cells," *Centre for VLSI and Embedded System Technologies (CVEST)*, pp. 735-738.

[5] D.Wang, M.Yang, W.Cheng, X.Guan, Z.Zhu, Y.Yang, "Novel Low Power Full Adder Cells in 180nm CMOS Technology," in *Prod. IEEE ICIEA* 2009, pp. 430-433.

[6] H. T. Bui, Y. Wang and Y. Jiang, "Design and Analysis of Low Power 10-Transistor Full Adders Using Novel XOR-XNOR Gates," IEEE Transactions on Circuits and Systems-II, Vol. 49, No. 1, Jan 2002, pp.25-30.