Design of Logical Effort for Worst Case Power Estimation in a CMOS Circuit in 90 nm Technology

Sachin Maheshwari[1], Amitoj Singh[1] and Dr. Anu Gupta[2]
Electrical and Electronics Department.
Birla Institute of Technology and Science,
Pilani-333031, District Jhunjhunu, Rajasthan, India.
sachin.mahe@gmail.com, amitoj14singh@gmail.com, anug@bits-pilani.ac.in

***Abstract*- The Logical Effort model is mainly to reduce delay in a circuit, but does not show how to minimize power and area. This paper deals with an empirical modeling and design of logical effort for estimating power in CMOS logic gates. The power is estimated in a circuit using the power of standard inverter and the relationship established between Power (P) and Logical Effort (g), Electrical Effort (h) and Parasitic (p) have been proposed in this paper. To verify the above model a full adder circuitry producing just the carry-out in UMC 90nm CMOS technology having supply voltage of 1V is selected. The results obtained from the model are accurate to 85.5% of the values obtained. The tool used is cadence and the simulation is performed using spectre.**

***Keywords:* logical effort, power estimation, modeling, CMOS logic gates, electrical effort, parasitic.**

I. INTRODUCTION

Power efficient is one of the key goals and among the most challenges in the design of deep sub-micron VLSI circuits and system [1]. CMOS technology scaling is mainly focused on high-performance and high speed circuits for ultra-low power applications. In these types of applications, the supply voltage is reduced well below threshold voltage of MOS devices in order to limit dissipation and to control the device leakage current due to the sub-threshold channel residual current. However, a trade-off exists in the design of high-performance, low-power, and reliable digital systems in presence of process variations [2]. Oklobdzija et. al [3] has successfully shown the performance comparison of VLSI adder using logical effort. Not only this, he has several papers on Energy minimization via circuit sizing [4] [5] [6] [7] [8].

The method of Logical Effort is an easy and widely used way to estimate the delay in a CMOS circuit [1], [5].Moreover, timing optimization methods typically lead to excessive power as a trade-off between the circuit speed and power dissipation. Kolodny et. al [9] extended the commonly used logical effort theory to model power as well as delay. Other approaches employ power-reducing design techniques via gate sizing and multiple threshold voltages [10] [11] [12] [13] [14].

In this paper a novel technique of finding the worst case total power P using the parameters logical effort(g), electrical effort (h) and parasitic (p) has been developed and later the devised technique is applied to a circuit to verify the results found. The paper is organized as follows: section II briefly explains the gate-delay model using logical effort; section III discusses the mobility ratio in 90nm technology node; section IV describes how to design logical effort for estimating power; section V explains the implementation of the devised relation on a more complex circuitry; and finally section VI concludes the analysis.

II. LOGICAL EFFORT MODEL

Logical effort is a design methodology for estimating the delay of CMOS logic circuits[15]. By comparing delay estimates of different logic structures, the fastest candidate can be selected. The method also specifies the proper number of logic stages on a path and the best transistor sizes for the logic gates.

Table I Equations of logical effort

Delay expression	$d = gh + p$
Absolute delay	$d_{abs} = d \times \tau$
Effort delay	$f = g \times h$
Logical effort	$g = \frac{C_{in}}{C_{inv}}$
Electrical effort	$h = \frac{C_{out}}{C_{in}}$
Path logical effort	$G = \prod g_i$
Branching effort	$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$
Path branching effort	$B = \prod b_i$
Path effort	$F = GBH$
Path delay	$D = \sum d_i = \sum g_i h_i + \sum p_i$
Minimum delay condition	$f' = g_i h_i = \sqrt[N]{F}$
Minimum path delay	$D = N \times \sqrt[N]{F} + P$
Best number of stages	$N = \log_4 F$

For proper understanding and further reading of this paper the reader should be familiar with the logical effort methodology [15]. Some of the logical effort equations that provide a way to determine appropriate transistor size of the critical path to minimize delay is tabulated in table I.

III. FINDING THE MOBILITY RATIO

According to Sutherland and Sproull [15] (1991, 1999) the mobility ratio of NMOS to PMOS transistor is 2:1. Using this knowledge, a simple CMOS inverter is implemented in 90nm to find the mobility ratio. The NMOS width of the inverter is taken as 1µm while keeping the lengths, for all transistors, as minimum. To calculate the PMOS transistor width (W_p), a relationship between the driving strength of PMOS and NMOS transistor is found, for a minimum delay. The value of W_p, where both high-to-low propagation delay (τ_{phl}) and low-to-high propagation delay (τ_{plh}) were equal, give the mobility ratio (NMOS to PMOS) for 90nm. Table II shows the delay at different width of PMOS while the width of NMOS (W_n) is kept constant as 1µm.

TABLE II. Delay at different PMOS width for static CMOS.

PMOS width (µm)	Low to high propagation delay (ns)	High to low propagation delay (ns)	Average propagation delay (ns)
1.5	23.73	9.64	16.685
1.7	21.1	9.95	15.525
1.9	18.96	10.2	14.58
2.1	17.27	10.56	13.915
2.3	15.64	10.71	13.175
2.5	14.3	10	12.15
2.7	13.4	11.15	12.275
2.9	12.53	11.5	12.015
3.125	12	12	12

IV. THE LOGICAL EFFORT MODEL FOR POWER CALCULATION

A static CMOS gate does not dissipate power during the absence of transients on the input: when the input is at high level (V_{dd}), only the NMOS transistor conducts, and when the input is at low level, only the PMOS will conduct. However, during a transient' on the input, there will be a time period in which both the NMOS and PMOS will conduct, causing a short-circuit current to flow from supply to ground. These currents flow as long as the input voltage (V_i) is higher than a NMOS threshold voltage (V_{tn}) and lower than a PMOS threshold ($|V_{tp}|$) below V_{dd} [4].

If the inverter output is loaded with a capacitance C_L, as shown in fig. 1, then the dissipation of the circuit consists of two components:

dynamic dissipation:

$$P_d = C_L \times V^2 \times f \qquad (1)$$

short circuit dissipation:

$$P_{sc} = I_{mean} \times V \qquad (2)$$

Where, V value of the maximum swing voltage available at the output and I_{mean} is the mean short circuit current flowing during the transition.

The power dissipated was calculated for a complete cycle of a pulse input of 1µs time period. The pulse has a 50% duty cycle and negligible slope of transition. The same input was applied to all the circuits to prevent an ambiguity in results due to difference in input signal. An inverter as shown in fig. 1 having minimum size MOSFET's and a C_L of 300fF at the V_{out} node was used as a reference for the development of the model. The power dissipated in this inverter for the period of pulse is 1.21 µW. The size of the MOSFET's in this inverter is the smallest possible for 90nm technology.

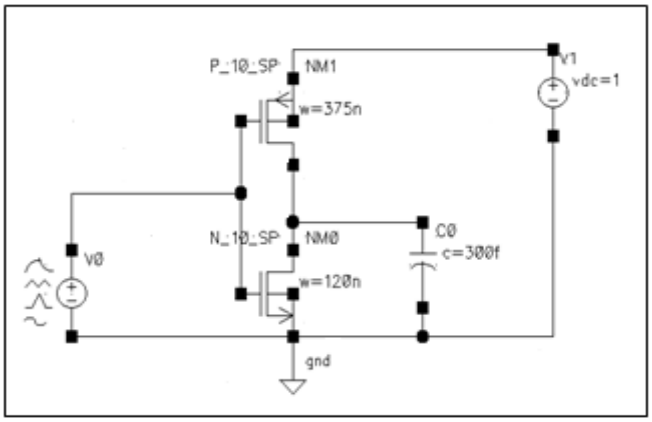

Figure 1. The inverter used as a standard for the development of the model

A. *Power vs. g(logical effort)*

To find about the dependence of logical effort the configuration of fig. 1 was changed, while keeping the functionality of the inverter. Thus, the input capacitance (C_{in}) changes, as the size of the MOSFET's is different but along with this, the logical effort (g) and electrical effort (h) also changes. To keep the h value as constant so as to capture only the effect of g the C_{out} is also changed which is shown in fig. 2.

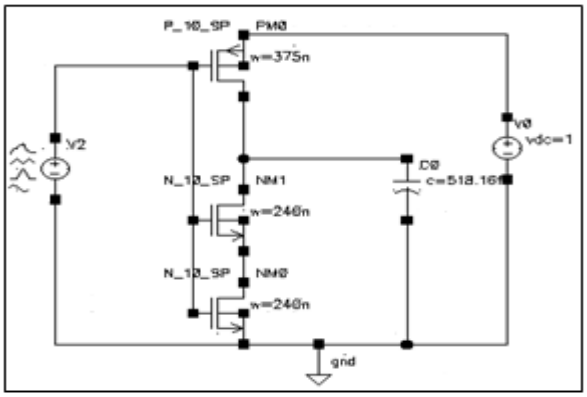

Figure 2. Inverter with series NMOS configuration.

$$g_1 h_1 = \frac{C_{out1}}{C_{inv}} \qquad (3)$$

since, $g_1 = 1$

$$h_1 = \frac{C_{out1}}{C_{inv}} \qquad (4)$$

Where, g_1 and h_1 are the logical and electrical efforts and C_{out1} is the output load capacitance of fig. 1. Similarly, for fig. 2

$$g_2 h_2 = \frac{C_{out2}}{C_{inv}} \quad (5)$$

$$g_2 = \frac{C_{in2}}{C_{inv}} \quad (6)$$

Where, C_{in2}= 375+240+240 and C_{inv}=375+120

g_2 comes out to be 1.7272. Thus, a change in C_{in} cause a change in g. Now, the condition for h to be constant is:

$$h_1=h_2 \quad (7)$$

taking equation 4 and 5

$$C_{out2} = g_2 \times C_{out1} \quad (8)$$

Thus, equation 8 shows that, to prevent a change of h the C_{out} is made 1.7272 times of the initial value. The power dissipated was calculated for fig. 2 which comes out to be 1.423µW.

It was observed that the inverter with C_{out} =300fF and having minimum sized MOSFET's as standard has power 1.21µW. The other inverter with C_{out}=518.16fF, having different configuration from the standard inverter has power 1.423µW. It can easily be found that;

$$\frac{P_2}{P_1} = \sqrt[0.29]{\frac{g_2}{g_1}} \quad (9)$$

With similar calculations of the power of G with which power varies and taking the average of such calculations the relation between P and g was found.

$$P = \sqrt[0.29]{g} \quad (10)$$

The table shows the varying power for 2 inverters. 1 being the reference and 2 being the inverter with different configuration and hence a different g. P_2/P_1 is directly proportional to g_2/g_1 to the power N. The average of N is 0.285.

TABLE III The change in power for constant change in g.

C_1(fF)	C_2(fF)	g_2/g_1	P_2/P_1	N
200	345.44	1.7272	1.1475	0.25175
225	388.62	1.7272	1.15577	0.265
250	431.8	1.7272	1.1632	0.2766
275	474.98	1.7272	1.17	0.2873
300	518.16	1.7272	1.1761	0.2968
325	561.34	1.7272	1.1815	0.305
350	604.52	1.7272	1.18638	0.3127

B. Power vs. h(electrical effort)

Another factor which changes the power is the change in h. Hence, the effect of change of h is captured by changing the output load, C_{out}, while the size of the MOSFET's is kept constant, which keeps input capacitance, C_{in} , to be constant. With change in C_{out} the factor logical effort, g, and parasitic, p, remain constant and hence the change in power is only due to the change in h value. The capturing of the effect of electrical effort (h) is shown in table IV, where the C_{out} is changed.

Where, h_1 and h_2 are the electrical efforts for reference inverter of fig.1 and fig. 2.

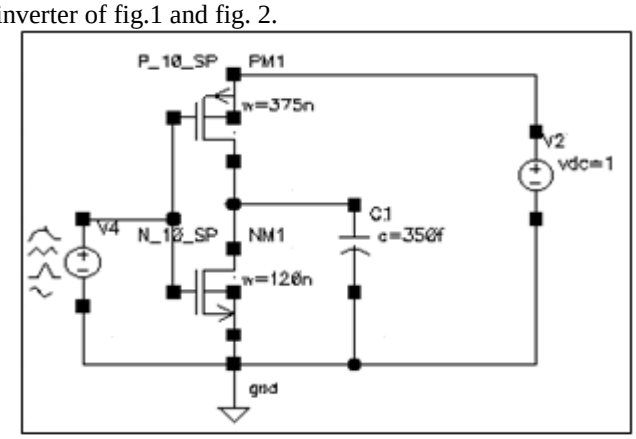

Figure 3. Circuit with h_2=1.167*h_1 of standard inverter

TABLE IV Power and Electrical effort for different load.

C_{out} (fF)	h(electrical effort)	(P)Power(µW)
200	5.991612	1.102
250	7.489515	1.1635
300	8.987418	1.21
350	10.48532	1.259
400	11.98322	1.305
450	13.48113	1.35
500	14.97903	1.394
550	16.47693	1.435
600	17.97484	1.4756

The change in electrical effort, h also cause power to change as shown in table IV. From the above table we can see that the power becomes 1.04 times, when the h is 1.167 times. The power in this case changes by a power of 0.26 of h. Thus, taking average of such similar cases the average power was found to be;

$$P = \sqrt[0.29]{h} \quad (11)$$

And hence, the expression now expanded to;

$$P = \sqrt[0.29]{gh} \quad (12)$$

C. Power vs. p(parasitic capacitance)

The principal contribution to the parasitic capacitance is the capacitance of the diffused regions of transistors connected to the output signal. Parasitic for any gate is defined as;

$$p = \left(\frac{\sum w_d}{1+\mu_n/\mu_p} \right) p_{inv} \quad (13)$$

Where, w_d is the width of transistors connected to the logic gate's output. p_{inv} is the parasitic for reference inverter which is taken to be 1.

The parasitic delay or simply the parasitic, p, give us a measure of the intrinsic capacitance of the gate present by virtue of the size of the MOS transistors. The parasitic vary linearly with the size of the MOS transistors [13]. Doubling the

size of all the MOSFET's present in a gate would approximately double the parasitic present. Usually the smallest size inverter has minimum parasitic and hence the value of p_{inv} for reference inverter is taken to be 1 and the rest are calculated according to this assumption.

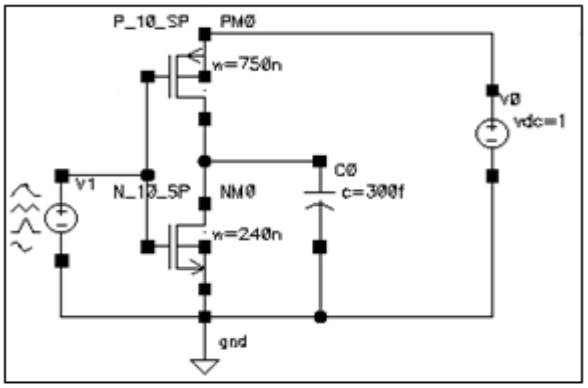

Figure 4. Inverter whose width are twice as that of reference inverter.

The only effect remaining is the parasitic capacitances, p which changed the power other than g and h. To find out how much power changed with change in P the widths of NMOS and PMOS transistors, W_n and W_p, are changed while keeping the required mobility ratio of NMOS and PMOS, μ_n/μ_p, (which was found to be 3.125 for 90nm technology). Changing the widths changes the C_{in} of the inverter which in turn changes both g and h, but gh product, which is C_{out}/C_{inv} remains constant, hence, the only change in power is due to the change in parasitic in such cases, as shown in Fig. 4.

The parasitic for fig. 4 was found using equation 13 and it comes out to be 2. p=2 means that the size of the NMOS and PMOS is double of the reference inverter. The power corresponding to it is 2.0127µW. The average change in power was found to be around 0.75 µW with unit change in p, as shown in table V.

Table V. The variation of p and the corresponding change in power.

Parasitic (p)	(P) Power (µW)
1	1.21
2	2.0127
3	2.8
4	3.583
5	4.3468
6	5.073556

Thus, the change in power varies linearly with an unit change in parasitic capacitance, p. We have now reached to a position where we could estimate the power that would be dissipated in a circuit using the power of reference inverter and the relation we had established between power (P), logical effort (g), electrical effort (h) and the parasitic capacitance (p).

V. THEORETICAL POWER ESTIMATION AND COMPARISON TO SIMULATED VALUE

The power estimation can be made using the logical effort model designed in the previous section. The model was tested on the circuit for carry output of full adder as shown in the Fig. 5. The maximum power dissipated in the circuit for output transition from 0-1 is about 8.26 µW. All the other input transition causing a similar low to high transition is lower than this value. The minimum power simulated was about 2.66 µW. Table VI shows the transitions of the input and the corresponding power dissipated in the circuit.

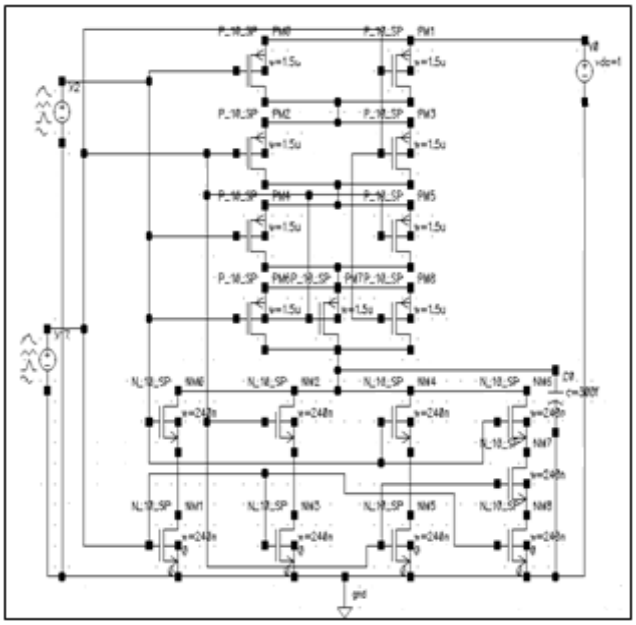

Figure 5. The circuit used for verification of the model

Table VI. Input transitions for the carry out calculator circuit and the corresponding power dissipated

ABC	A'B'C'	(P) Power (in µW)
011	000	8.26
111	000	7.92
101	100	5.5
011	100	4.2797
011	001	4.02
011	010	3.93
110	100	2.66

Although the calculations remain the same for all the inputs, in fig. 5 the calculations of g and h were done considering C_{in} as the input. The gh product for the fig. 5 is the same as for a reference inverter. The only difference between the two circuits is the C_{in} which cancels out when the product of gh is taken. Hence the only change in power in the above circuit when compared to the reference would be due to the parasitics. According to the relation between Power and p, the power changes by 0.7-0.8 µW for each unit change in p.

The p of fig. 5 is about 11 times than that of the reference inverter which implies that the power of fig. 5 should be 8.25µW more than the reference inverter. If the power consumption of the standard inverter is 1.21 µW the power consumption of the above circuit will be around 9.46 µW. This meant that by using power dissipated in a reference circuit and the dependence of power on g, h and p parameters worst case power for a circuit can be predicted with 85.5% accuracy.

VI. CONCLUSION

In this paper an empirical model for the worst case power estimation of any logical circuit using a reference circuit and the logical effort parameters g, h and p has been presented. The accuracy of this model is about 85.5%. Power was found to be directly proportional to $(gh)^{0.29}$, also the power increased by 0.75µW with a unit increase in parasitic (p). This empirical model can be expanded to a chain of such circuits as most of the circuits used are used as a part of a chain. Also the model could be tested for other technologies and a link between the factors found for different technologies may also be established.

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