Analysis of 20nm SOI MOSFET SRAM Design Using Different Gate Materials

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Abstract- **The SOI MOSFET technique is used to overcome the scaling effects. In this work, 20nm SOI MOSFET using Poly silicon as gate material of both N-type and P-type were designed. The same SOI MOSFET is designed using Molybdenum as gate material for both N-type and P-type and the device characteristics werecompared and analysed.**

Keywords:**SOI-Silicon On Insulator, SNM-Static Noise Margin, S-Sub threshold Slope**

I INTRODUCTION

MOSFET is considered as backbone of electronics. Ingenious engineering has allowed its size to be shrunk again and again without change to its structural design. Yet the IC design window of performance, dynamic power, static power, and device variation has shrunk to the point that major investment for a new transistor structure can be justified. As gate length shrinks, MOSFET's Id-Vg characteristics degrade in two major ways. First the sub threshold swing degrades and Vt decreases, i.e. the device cannot turned off by lowering Vg easily. Second, S and V_t become increasingly sensitive to Lg variations, i.e. device variations become more problematic. **All these problems may be called the short-channel effects**[1].

A transistor is turned on and off when Vg lowers and raises the potential of the channel (and thus the potential barrier between the channel and the source) through the gate to channel capacitance, Cg. In an ideal transistor, the channel potential is only controlled by Vg and Cg. In a real transistor, the channel potential is also subject to the influence of $V_d$through Cd. When Lg is large, Cd is much smaller than Cg and the drain voltage does not interfere Vg's role as the sole controlling voltage. As Lg decreases, Cd increases (exponentially [2]) and Vg loses its absolute control over the on-off states of the transistor. In the extreme case, Vg has little control and the transistor can be turned on by V_d alone without Vg. Before reaching that extreme, $V_t$decreases with increasing Vd and decreasing Lg and S becomes large. The solution is to increase Cg by using high-k gate dielectric and metal gate that eliminates the poly-gate depletion layer. SOI MOSFET provides very low junction capacitance i.e. the source and drain junction capacitance is almost entirely eliminated in SOl MOSFETs. The capacitance through the thick buried oxide layer to the substrate is very small. No body effect because of the threshold voltage of stacked devices in SOI [3].We choose a 20 nm device design according to the structure shownin Fig. 1. This work is organised as the designing techniques of the device in section III. The analysis of SOI MOSFET isdone in section IV. Finally the conclusion isdiscussed insectionV.

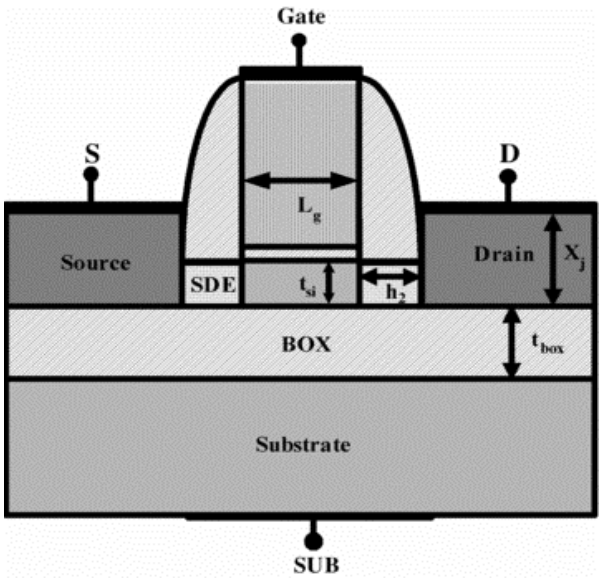


Figure1. Schematic view of 20nm SOI MOSFET.

II PREVIOUS WORK

CMOS in PD-SOI is easier to manufacture than in FD-SOI. On the other hand, unless the channel body is intentionally tied electrically to the source, e.g., [6], they exhibit marked floating-body effects. Of more significance for circuit operation are the dynamic floating-body effects which can be distinguished in two categories, capacitive, and bipolar turn-on. These effects affect the instantaneous value of V_{bs} and hence of the drain current. Capacitive effects arise from the capacitive coupling of the floating-body to the gate, source and drain. Contrary to bulk where body charge, Q_b, is free to move in the form of majority carrier current to or from rthe fixed-voltage body in response to gate, source, and drain voltages, in PD-SOI MOSFETS this charge is near-constant in the time-scale of typical logic clock frequencies and therefore V_{bs} has to vary in that time-scale [7] [8].PD-SOI CMOS can be built on a variety of different silicon film thickness. The disadvantage for this device type

comes from the floating-body effects which need to be carefully designed [9]. When the SOI silicon film thickness t_{si} is less than the depletion depth t_d, under the inversion channel, SOI MOSFETs are said to be fully depleted. They are attractive because of decreased floating-body effects, they are difficult to manufacture because they require very thin t_{si} in order to be truly free of these effects. For this reason a compromise between severity of floating-body effects and manufacturability dictates t_{si} values thicker than optimum [9].

III DEVICE DESIGN

SOI CMOS involves building more or less conventional MOSFETs on a thin layer of crystalline silicon. The thin layer of silicon is separated from the substrate by a thick layer (typically 100 nm or more) of buried Si02 film, thus electrically isolating the devices from the underlying silicon substrate and from each other. SOI CMOS process can be readily developed due to the compatibility with established bulk processing technology. In order to make the device compact 20nm technology is used. DESSIS simulator is used to simulate the 2D devices. The parameters are mentioned in table I.

Table I.FinFET Device Parameters

Parameters	Dimensions
L_g(nm)	20
t_{ox}(nm)	1.2
$N_{sub}(cm^{-3})$	10^{16}
$N_{sd}(cm^{-3})$	10^{20}
V_{dd}(V)	1.2

N_{sub}: Substrate doping concentration.
N_{sd}:Source/Drain peak concentration.
L_g: Gate length
t_{ox}: Gate oxide thickness
V_{dd}: Supply voltage

The gate materials used here areboth Polysilicon and Molybdenum. Table I is applicable for both N-type and P-type SOI MOSFET devices. The drive characteristics of both N-MOS and P-MOS were tabulated in table II. The work function of Polysilicon is 4.1eV and the work function of Molybdenum is 4.37eV. The metal gate has been used becauseas a work function of the material is high the performance of the device improves. Moreover the dopant penetration that occurs due to scaling is avoided by using metal gate and also the metals has low sheet resistance.

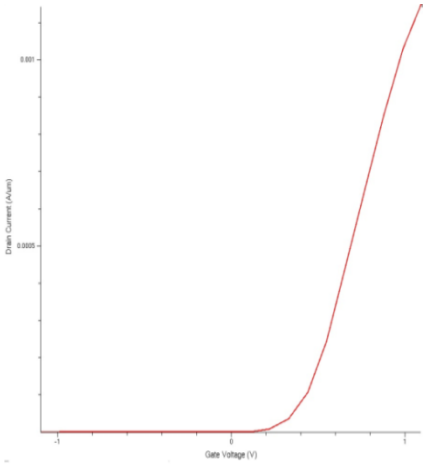


Figure2. ON-current for SOI N-MOSFET(Polysilicon)

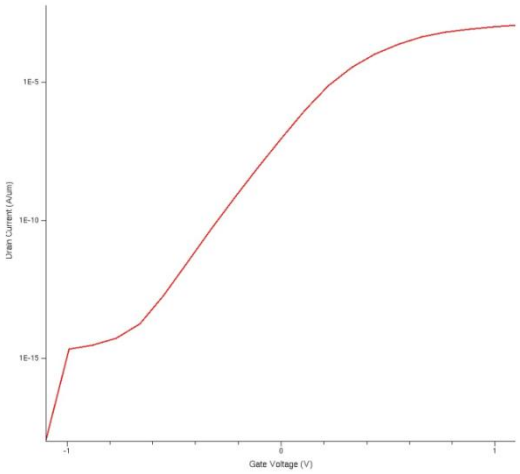


Figure3. OFF-current for SOI N-MOSFET (Polysilicon)

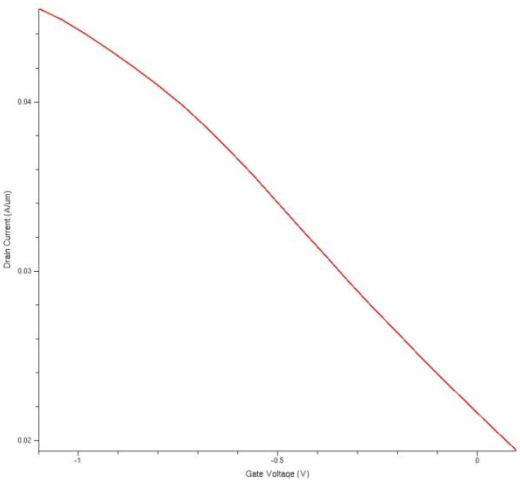


Figure4. ON-current for SOI P-MOSFET (Polysilicon)

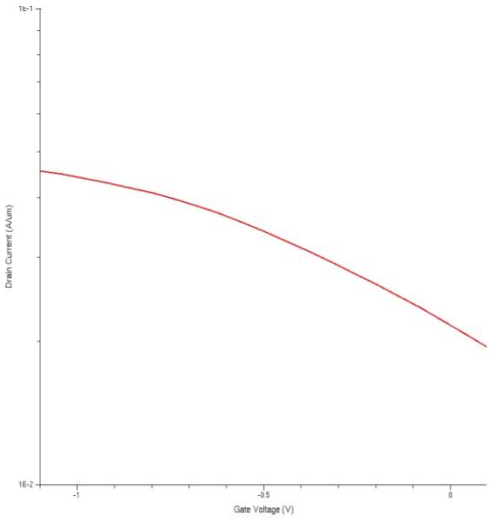


Figure5. OFF-current for SOI P-MOSFET (Polysilicon)

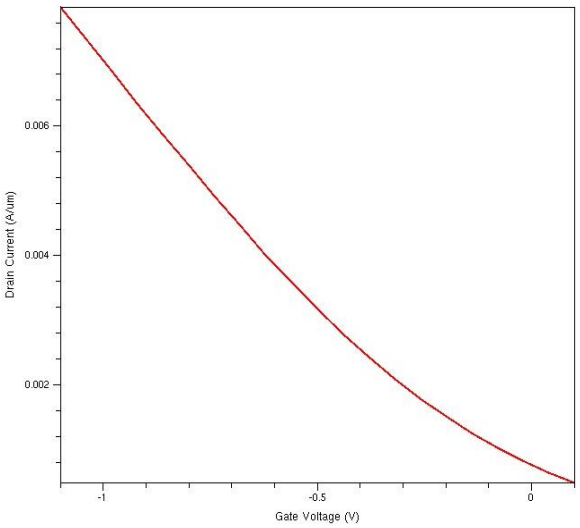


Figure8. ON-current for SOI P-MOSFET(Molybdenum)

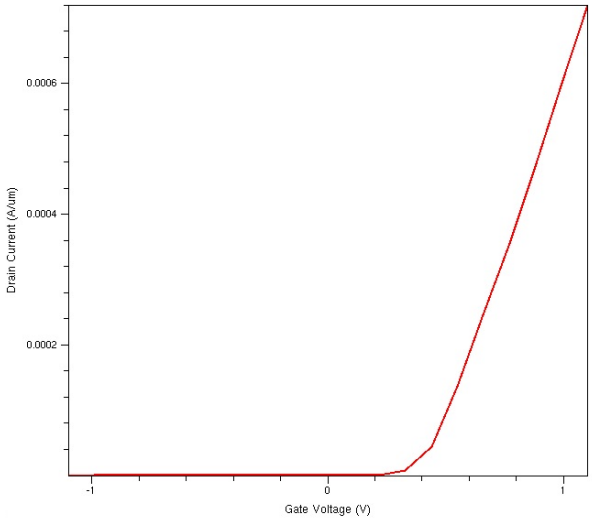


Figure6. ON-current for SOI N-MOSFET (Molybdenum)

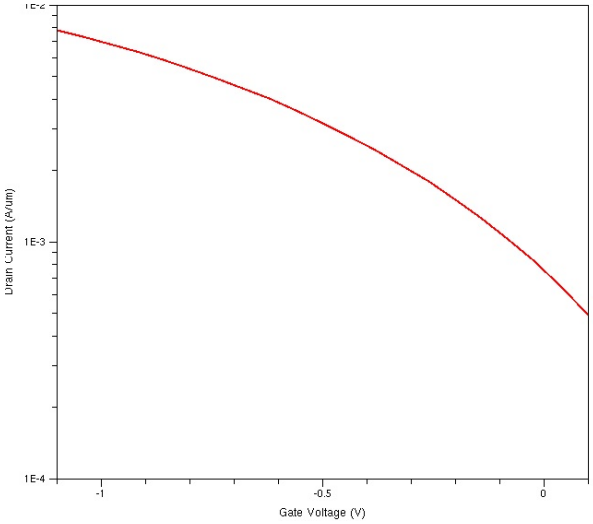
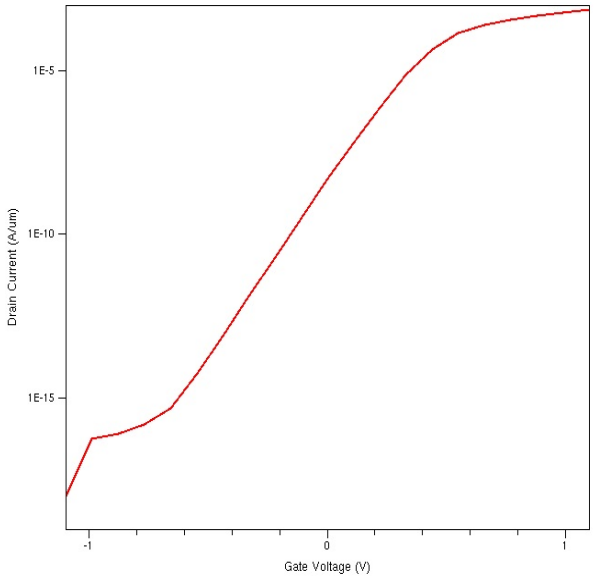


Figure9. OFF-current for SOI P-MOSFET (Molybdenum)



Figur7. OFF-current for SOI N-MOSFET (Molybdenum)

Table I. FinFET Device Parameters

Material	Type	Ion (A/µm)	Ioff (A/µm)	Ion/Ioff ratio
Polysilicon	N	1.158e-03	9.312e-08	1e+05
	P	4.553e-02	2.165e-03	1e+01
Molybdenum	N	7.204e-04	4.549e-09	1e+05
	P	7.844e-03	7.62e-04	1e+01

From the above tabulation it is shown that the SOI MOSFET has good Ion/Ioffratio, so it is clear that it has a fast transition so thereby this device enhance the read and write operation. The timing required for the

operation of the SRAM cell is less and it is applicable for high speed applications. Barrier lowering increases as channel length is reduced, even at zero applied drain bias, because the source and drain form pn junctions with the body, and so have associated built-in depletion layers associated with them that become significant partners in charge balance at short channel lengths, even with no reverse bias applied to increase depletion widths. But as metal gate is used DIBL is low which in turn results in low leakage and hence applicable for low power applications.

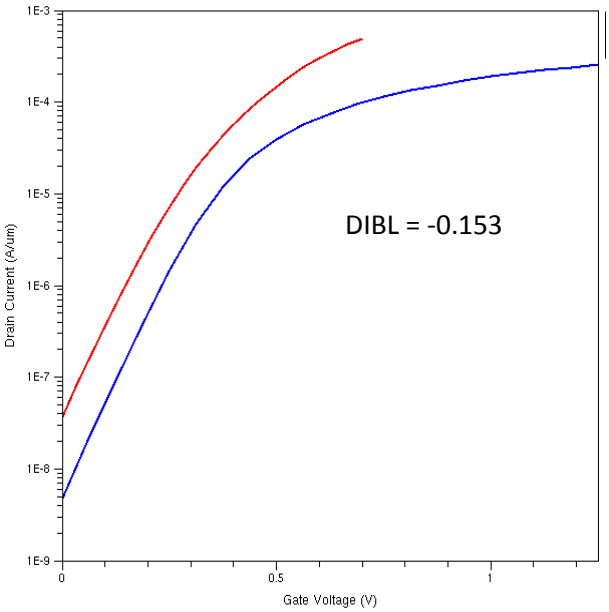


Figure10. DIBL for Polysilicon MOSFET

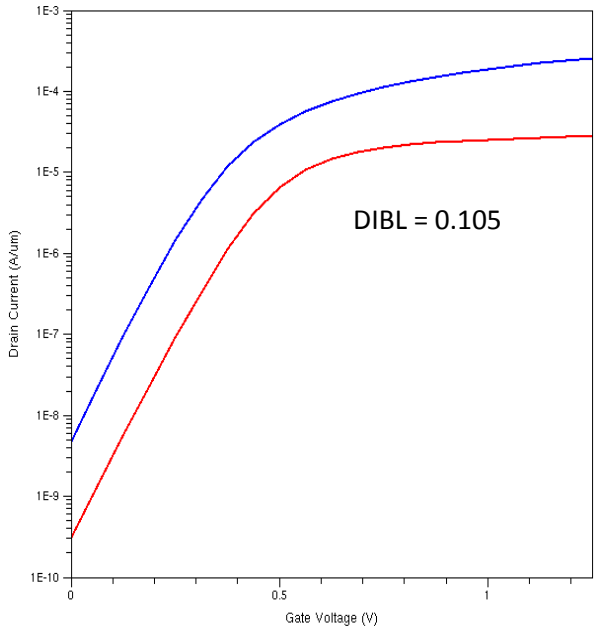


Figure11. DIBL for Metal Gate MOSFET

IV ANALYSIS OF SOI MOSFET SRAM

Vast resources have been expended by the semiconductor industry trying to build a non-volatile random access read/write memory[4]. The effort has been undertaken because non-volatile RAM offers several advantages over other memory devices DRAM, Static RAM, Shadow RAM, EEPROM, EPROM and ROM—which were developed to meet specific applications needs.Characteristics of the Static RAM over other RAMs are: low power consumption, high performance, high reliability, high density, low cost,and the ability to be used in any semiconductor memory application.An SRAM is essentially a stable DC flip-flop requiring no clock timing or refreshing. The contents of an SRAM memory are retained as long as power is supplied. SRAMs support extremely fast access times. SRAMs also have relatively few strict timing requirements and a parallel address structure, making them particularly suited for cache and other low-density, frequent-access applications [5].

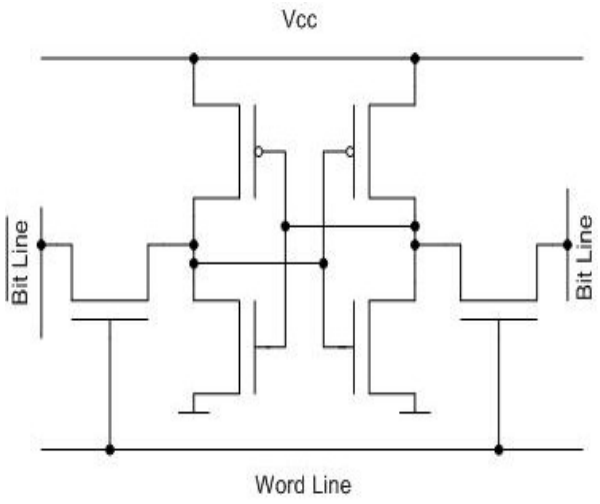


Figure12. Schematic view of 6-T SRAM cell

In this section, existing static approach that is butterfly method for measuring static noise margin is discussed. Static noise margin of the SRAM cell depends on the cell ratio (CR), supply voltage and also pull up ratio. For stability of the SRAM cell, good SNM is required that is depends on the value of the cell ratio, pull up ratio and also for supply voltage. Driver transistor is responsible for 70 % value of the SNM.

SNM, which affects both read margin and write margin, is related to the threshold voltages of the NMOS and PMOS devices in SRAM cells. Typically, to increase the SNM, the threshold voltages of the NMOS and PMOS devices need to be increased. However, the increase in thresholdvoltage of PMOS and NMOS devices is limited. The reason is that SRAM cells with MOS devices having too high threshold voltages are difficult to operate; as it is hard to flip the operation of MOS devices.

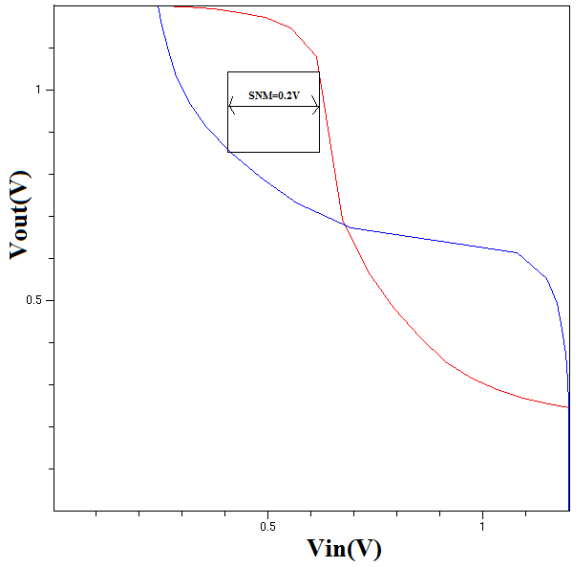


Figure13. SNM plot for 6-T MOSFET (Polysilicon)

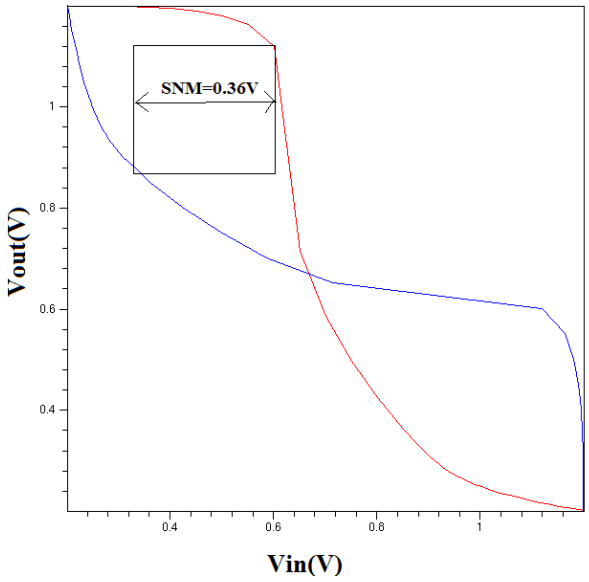


Figure14. SNM plot for 6-T MOSFET (Molybdenum)

V. CONCLUSION

While taking the DIBL effect into consideration, results shows that metal gate has low value so its suitable for low power applications. The value of SNM for SOI MOSFET (Polysilicon) is found to be 0.2V, Fig 13 and the value of SNM for SOI MOSFET (Molybdenum) is found to be 0.36V, Fig 14. This proves that the metal gate SOI MOSFET is less prone to noise. The device has good Ion/Ioff ratio, this enhances the operation speed of the SRAM cell and hence can be used in high speed applications. From the above discussions it is clear that this 20nm SOI MOSFET is applicable in low power and high speed applications.

VI REFERENCES

[1]Fundamentals Of Modern" VLSI Devices second edition Yuan TaurUniversity of California, San Diego Tak H. NingIBM T. J. Watson Research Center, New York.
[2] Z. Liu et al. IEEE Transaction on Electron Devices pp. 86-95, Jan. 1993.
[3] Fundamentals of Modern" VLSI Devicessecond edition Yuan TaurUniversity of California, san Diego Tak H. NingIBM T. J. Watson Research Center, New York.
[4] MAXIM – Mar 29, 2009
[5] www.itrs.com
[6] D. Suh and J. G. Possum, IEEE Trans. Elec. Dev., vol.42, no. 4, 1995, pp.728-737.
[7] A. Wei et al., IEEE Electron Dev. Lett., vol. 17 , no. 8, 1996, pp. 391-394.
[8] J. Gautier et al., in Int. Electron Devices Meeting (IEDM) Tech. Dig., 1995, pp.623-626.
[9] SOI CMOS as a mainstream low-power technology: A critical assessment by Dimitri A. Antoniadis